IEEE SOLID-STATE CIRCUITS SOCIETY / UNIVERSITY OF PENNSYLVANIA

ADVANCE PROGRAM

2008 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 3, 4, 5, 6, 7

CONFERENCE THEME:

System Intergration for Life and Style

SAN FRANCISCO MARRIOTT HOTEL

5-DAY PROGRAM

SUNDAY ALL-DAY: 3 FORUMS: Embedded Memory; Wide-DR Imaging; GIRAFE: Nanoscale RF CMOS — 10 TUTORIALS — 2 SPECIAL-TOPIC SESSIONS: Green Electronics ; MEMS for Frequency Synthesis and Wireless RF

THURSDAY ALL-DAY: 4 FORUMS: GW to µW Power Systems; High Speed Transceivers; Transistor Variability; Digitally-Assisted Analog and RF — SHORT-COURSE: Power Mangement

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency and to network with leading experts.

CONFERENCE HIGHLIGHTS

On **Sunday, February 3rd**, the day before the official opening of the Conference, ISSCC 2008 offers:

- A choice of up to 4 of a total of 10 Tutorials
- Three ISSCC Advanced Circuits Forums:
  - GIRAFE (GHz Radio Front Ends): Architectures & Circuit Techniques for Nanoscale RF CMOS
  - Memory Circuit Design Forum: Embedded Memory for Nano-Scale VLSI Systems
  - Imager Forum: Wide-Dynamic Range Imaging

The 90-minute tutorials offer background information and a review of the basics in specific circuit design topics. In the all-day Advanced Circuit Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday evening, two Special-Topic Evening Sessions addressing next-generation circuit-design challenges will be offered starting at 7:30PM:

- Green Electronics – Environmental Impacts and Power eWaste
- MEMS for Frequency Synthesis & Wireless RF Communications

The Special-Topic Evening Sessions are open to all ISSCC attendees.

On **Monday, February 4th**, ISSCC 2008 offers four plenary papers followed by six parallel technical sessions. A Social Hour open to all ISSCC attendees will follow the afternoon session. The Social Hour will feature posters from the winners of the 2008 joint DAC / ISSCC student design contest and the 2007 Asia Solid-State Circuits Conference student design contest. Monday evening features a panel discussion "Private Equity: Fight Them or Invite Them" and three Special-Topic Evening Sessions:

- From Silicon to Aether and Back
- Data Converter Directions
- Trusting our Lives to Sensors

On **Tuesday, February 5th**, ISSCC 2008 offers morning and afternoon technical sessions, followed by a Social Hour, an evening panel; "Can Multicore Integration Justify the Increased Cost of Process Scaling" and two Special-Topic Evening Sessions:

- Trends and Challengers in Optical Communications Front-End
- Highlights of IEDM 2007

Today a Luncheon for Women in Solid-State Circuits will be held in the View Lounge.

Wednesday, February 6th features morning and afternoon technical sessions.

On **Thursday, February 7th**, ISSCC 2008 offers a choice of four events:

- An ISSCC Short Course: "Embedded Power Management for IC Designers". Two sessions of the Short Course will be offered, with staggered starting times.
- Four ISSCC Advanced Circuits Forums:
  - Power Systems from Gigawatts to Microwats
  - Future of High-Speed Transceivers
  - Transistor Variability in Nanometer-Scale Technologies
  - Digitally-Assisted Analog and RF Circuits

Registration for educational events will be filled on a first-come, first-served basis. Use of the ISSCC web-registration site (www.isscc.org) is strongly encouraged. You will be provided with immediate confirmation on registration for Tutorials, Advanced Circuit Design Forums and the Short Course.

This year, for the first time, attendees will be able to register for unlimited on-demand web access to multi-media replay of ISSCC technical papers. Attendees will be able to listen to papers they could not attend or to re-play a paper they attended for better understanding.

T1: Fundamentals of Class-D Amplifier Operation & Design
Class-D amplifiers, due to their high efficiencies, are extremely attractive for integrated and low power applications where long battery life and reduced heat are crucial. This tutorial begins with a brief overview of architectures and system concerns and is followed by detailed explanations of the issues found in the typical class-D design process. We will conclude with some insights into the current state of the art as well as what the future might hold in this area.

Instructor: Brett Forejt graduated from Carnegie Mellon University in 1995 with his BSEE and graduated from Oregon State University in 1998 with his MSEE. Brett has over 12 years of industry experience in analog and mixed-signal design starting in 1995 with Hewlett Packard. In 1997, he joined Texas Instruments working in wireless telephony. Brett continues to work for Texas Instruments in the High-Performance Analog Division, in the Audio & Imaging Products group where he is a Senior Member Technical Staff. Brett is a Senior Member of IEEE and has served on the ISSCC analog subcommittee since 2005.

T2: Pipelined A/D Converters: The Basics
For resolutions from 8- to 14-bits at speeds from 1MS/s to greater than 1GS/s, pipelined ADCs have become the ADC architecture of choice. This tutorial starts with the basics. A spatial analogy is used to explain sub-ranging and redundancy leading to a simple intuitive understanding of all such architectures, including non-radix-two successive approximation ADCs. Key circuit-design issues will be addressed, such as amplifier requirements and device sizing for noise and matching constraints. These concepts will then be applied in the context of a generic design example of a 10-bit ADC.

Instructor: Aaron Buchwald is currently CEO and co-founder of Mobius Semiconductor, a privately held start-up in Irvine, CA. He has 25 years experience in the field of analog integrated circuit design. Dr. Buchwald joined Broadcom in 1994 as the first member of the analog group, where he was the lead designer for several generations of ADCs and front-end circuitry for products in the cable, satellite and networking markets. He was later responsible for development of multi-gigabit serial transceivers for XAUI, CX4 and Fiber Channel. Dr. Buchwald was formerly an Assistant Professor at the Hong Kong University of Science and Technology (HKUST). Prior to that he worked at Siemens in Munich, Germany and Hughes Aircraft in El Segundo, CA. Dr. Buchwald has a BSEE from the University of Iowa, and an MS and PhD from the University of California, Los Angeles. He is Co-author of the book *Integrated Fiber-Optic Receivers*, Kluwer, 1995 and was the co-recipient of the ISSCC outstanding-paper award in 1997 for the design of a 10-bit video-rate data converter.

T3: CMOS Temperature Sensors

CMOS temperature sensors are everywhere! They are used in CPUs for thermal management, in DRAMs to control refresh rates, and in MEMS frequency references for temperature compensation, to name a few high-volume applications. In this tutorial, the operating principles of CMOS temperature sensors will be explained, their main sources of inaccuracy identified, and suitable remedies, at the device, circuit and system levels, described. To further illustrate these concepts, the design of a state-of-the-art CMOS temperature sensor with an inaccuracy of less than 0.1°C over the military temperature range (–55°C to 125°C) will be presented.

Instructor: Kofi A.A. Makinwa is an Associate Professor at Delft University of Technology, The Netherlands, where he leads a group that designs precision analog circuits, ΔΣ modulators, and smart sensors. He holds B.Sc. (1st Class Hons.) and MSc degrees from Obafemi Awolowo University, Nigeria, an MEE (*cum laude*) degree from the Philips International Institute, The Netherlands and a PhD degree from Delft University of Technology. From 1989 to 1999 he was a research scientist at Philips Research Laboratories, after which he joined Delft University of Technology. He holds nine U.S. patents, has (co)-authored over 60 technical papers, and has given tutorials at several conferences, including the ISSCC. Dr. Makinwa is a (co)-recipient of JSSC, ISSCC and ESSCIRC outstanding paper awards, a recipient of the Veni and Simon Stevin Gezel awards from the Dutch Technology Foundation, and a member of the Young Academy of the Royal Netherlands Academy of Arts and Sciences.

T4: SoC Power-Reduction Techniques

Power consumption is and continues to be the hottest topic for battery-operated portable devices. This tutorial provides a comprehensive overview of most commonly adopted Digital CMOS Leakage Reduction and Power-Management techniques. It also presents the benefits of those techniques and their realization at all phases of the IC design process, from system architecture to physical implementation. What is DVFS? What does power gating mean? How can massive clock gating help to reduce leakage? How to apply low power techniques to SRAM design? How can system architectures help? These are among the questions that will be answered during this tutorial.

Instructor: Pascal Urard is currently High-Level Synthesis manager at STMicroelectronics in Crolles, France. He is involved in the design of high-performance and low-energy solutions for applications in digital communications and multimedia, with a special focus on high-speed wireless communications. He received his MS in Electronics Engineering from the ISEN (Institut Supérieur d'Electronique du Nord), located in Lille, France, in 1991. He has published 13 IEEE papers, has 10 awarded or pending patents in the domain of signal processing, and is regularly invited in panel sessions on System-Level Design. He recently joined TPC of IEEE conferences such as ISSCC, ESSCIRC and MEMOCODE. He is a technical adviser of few large EDA companies in System-Level Design.

T5: Digital Phase-Locked Loops

Phase-locked loop (PLL) circuits are a key component of most modern communication circuits, and are also used in a variety of digital processor applications in order to generate high-frequency low-jitter clock sources. Here, we examine the issue of achieving digital implementation of these structures with the aim of achieving excellent noise performance. Basic concepts of classical analog PLL structures will first be examined, followed by an overview of digital PLL structures and their associated circuit implementation issues. Higher level design and simulation techniques are presented, as well as several case studies of implemented examples.

Instructor: Michael H. Perrott received the BS degree in electrical engineering from New Mexico State University, Las Cruces, NM in 1988, and the MS and PhD degrees in electrical engineering and Computer Science from Massachusetts Institute of Technology in 1992 and 1997, respectively. From 1997 to 1998, he worked at Hewlett-Packard Laboratories in Palo Alto, CA, on high speed circuit techniques for ΔΣ synthesizers. In 1999, he was a visiting Assistant Professor at the Hong Kong University of Science and Technology, and taught a course on the theory and implementation of frequency synthesizers. From 1999 to 2001, he worked at Silicon Laboratories in Austin, TX, and developed circuit and signal processing techniques to achieve high-performance clock- and data-recovery circuits. He is currently an Associate Professor in electrical engineering and Computer Science at the Massachusetts Institute of Technology, and focuses on high-speed circuit and signal processing techniques for data links and wireless applications.

T6: Leakage-Reduction Techniques

CMOS technology scaling in sub-100nm range comes with increased transistor leakage. To continue harvesting technology scaling benefits, it is essential for circuit designers and system architects to understand the nature and impact of leakage, its sensitivity to different design parameters, and practical techniques to reduce it. This tutorial will review process and circuit design techniques for leakage reduction with examples from 65nm and 90nm designs from the industry as well as academic research. Special emphasis will be devoted to power gating techniques, the equivalent of clock gating for local leakage mitigation.

Instructor: Stefan Rusu received the MSEE degree from the Polytechnic University in Bucharest, Romania. His industry experience includes over 15 years with Intel and 6 years at Sun Microsystems. He is presently a Senior Principal Engineer in Intel's Enterprise Microprocessor Group leading the technology and special circuits design activities for the Xeon® MP Processors. He has authored over 75 papers on VLSI circuit technology and holds 30 U.S. patents. He is an IEEE Fellow, a member of the Technical Program Committee for ISSCC, ESSCIRC and A-SSCC conferences and an Associate Editor of the IEEE Journal of Solid-State Circuits.

T7: NAND Memories for SSD

The NAND-flash-memory-based solid-state disk (SSD) for PC applications has attracted a lot of attention as the cost of NAND flash memory drastically reduces. To realize a high performance and highly reliable SSD, it is essential to understand SSD from a broad perspective such as device, circuit, system architecture and operating system. This tutorial covers the following topics to provide a comprehensive view of SSD.

- NAND device/circuit basic operation
- SSD overview such as market, cost, reliability, performance, power consumption.
- NAND circuit design for SSD
- NAND controller design for SSD
- Operation system for SSD

Instructor: Ken Takeuchi is currently an Associate Professor at the Graduate School of Frontier Sciences and Electronics Engineering Department of the University of Tokyo. He is now working on VLSI circuit design especially on emerging non-volatile memories. He received the BS and MS degrees in Applied Physics and the PhD degree in electrical engineering from the University of Tokyo in 1991, 1993 and 2006, respectively. In 2003, he also received an MBA degree from Stanford University. Since he joined Toshiba in 1993, he has been leading Toshiba's NAND flash memory circuit design for fourteen years. He designed six of the world's highest-density NAND flash memory products such as 0.7μm 16Mb, 0.4μm 64Mb, 0.25μm 256Mb, 0.16μm 1Gb, 0.13μm 2Gb and 56nm 8Gb NAND flash memories. He holds more than 100 patents including 72 U.S. patents; especially notable is his invention of "multi-page cell architecture", presented at Symposium on VLSI Circuits in 1997, he successfully commercialized the world's first multi-level cell NAND flash memory in 2001. He has authored numerous technical papers, one of which won the Takuo Sugano Award for outstanding paper at ISSCC in 2007. He has served on the ISSCC Memory subcommittee since 2007.

T8: Silicon mm-Wave Circuits

A recent surge of interest in Si mm-wave circuits and systems, evidenced by the number of conference/journal papers and new research organizations, clearly demonstrates keen interest in exploring new applications for mm-wave frequencies. The design of circuits above 30GHz poses unique challenges and requires new design methodology, often outside the realm of the analog circuit designer's background and skill set. This tutorial will review fundamental theory and practical techniques applicable to mm-wave circuits. The design of key building blocks such as amplifiers, mixers, and oscillators will be discussed incorporating Si transmission-line techniques, matching circuits, and distributed elements.

Instructor: Ali M. Niknejad received the BSEE degree from the University of California, Los Angeles, in 1994, and the MS and PhD degrees in electrical engineering from the University of California, Berkeley, in 1997 and 2000. From 2000-2002, he worked in industry where he was involved with the design and research of CMOS RF integrated circuits. Presently he is an associate professor in the EECS department at UC Berkeley. He is a co-director of the Berkeley Wireless Research Center (BWRC) and also the co-director of the BSIM Research Group. He served as an associate editor of the IEEE Journal of Solid-State Circuits and is currently serving on the ITPC for ISSCC and CICC. His current research interests lie within the area of RF/microwave and mm-wave integrated circuits and device modeling.

T9: CMOS+Bio: The Silicon that Moves and Feels Small Living Things
Silicon microelectronic chips are emerging as powerful new tools for rapid, sensitive, and direct analysis of biological objects, *e.g.*, cells, proteins, viruses, and DNA. The interface between electronic and biological systems is aimed at revolutionary advances in human health care, *e.g.*, early disease detection. This tutorial attempts an effective exposure to this burgeoning field, discussing how to structure and design silicon ICs for front-end biosensing and actuation in direct contact with the biological world. Topics include CMOS magnetic-resonance biomolecular sensors, CMOS DNA microarrays, CMOS microarrays to detect proteins & viruses, CMOS cell actuators, and CMOS-neuron interfaces.

Instructor: Donhee Ham is John L. Loeb Associate Professor of Natural Sciences at Harvard University, where his research group works on: (1) RF & analog ICs; (2) ultra-fast quantum transports using low-dimensional nano devices; (3) soliton electronics; (4) applications of CMOS ICs in biotechnology. He received his BS degree in physics from Seoul National University, graduating atop the Natural Science College, and PhD degree in EE from Caltech, winning the Charles Wilts Prize, best-thesis award in EE. His work experiences include the Laser Interferometer Gravitational Wave Observatory, IBM T. J. Watson Research Center, IEEE technical program committees including ISSCC, and technical advisory positions on ultrafast solid-state electronics and science & technology at the nanoscale. He was a fellow of the Korea Foundation for Advanced Studies, a recipient of the IBM Doctoral Fellowship, and a recipient of the IBM Faculty Partnership Award. He is a co-editor of CMOS Biotechnology with Springer (2007).

T10: Basics of High-Speed Chip-to-Chip and Backplane Signaling
This tutorial presents the basics of high-speed transceivers with emphasis on circuit design requirements for chip-to-chip and backplane signaling. The topics include channel characterization and equalization, MUX and DEMUX design, decision circuits, as well as clock- and data-recovery (CDR) circuits and concepts. Approximately half of the tutorial will be devoted to I/O blocks and half to CDR. The goal of the tutorial is to help the audience absorb the related papers presented at the conference.

Instructor: Ali Sheikholeslami is an Associate Professor of ECE at the University of Toronto, Canada. His research interests are in the areas of high-speed signaling and VLSI memories. He spent the 2005-2006 academic year on research sabbatical with Fujitsu Labs of Japan and Fujitsu Labs of America, focusing on high-speed signaling circuits. Prof. Sheikholeslami has received several awards in teaching, including the ECE Department's Best Professor of the Year Award in 2000, 2002, and 2005, and the Faculty of Applied Sciences and Engineering's Early Career Teaching Award in 2006, all at the University of Toronto, Canada. He is a member of the ISSCC Program Committee, a senior member of the IEEE, and a registered professional engineer in the province of Ontario, Canada.

F1: Embedded Memory Design for Nanoscale VLSI Systems

Organizer: **Kevin Zhang,** *Intel, Hillsboro, OR*

Committee: **Mark Bauer,** *Intel, Folsom, CA*
Martin Brox, *Qimonda, Neubiberg, Germany*
Shine Chung, *TSMC, Hsinchu, Taiwan*
Hideto Hidaka, *Renesas Technology, Itami, Japan*
Peter Rickert, *Texas Instruments, Dallas, TX*
Ken Takeuchi, *University of Tokyo, Tokyo, Japan*
Hiroyuki Yamauchi, *Fukuoka Institute of Technology, Fukuoka, Japan*

Embedded memory plays a key role in achieving overall power and performance goal for VLSI systems. As technology scaling continues to drive higher level of integration in VLSI design for ever-increasing performance, embedded memory becomes even more critical in the era of nano-scale CMOS technology. In this Forum, a variety of embedded memories, including SRAM, DRAM, Flash, MRAM, and FeRAM, are discussed by industry experts in the fields. Key technical topics such as technology scaling, critical circuit design, and power management are presented along with product requirements for different applications.

Forum Agenda:

Time	Topic
8:00	Breakfast
8:20	**Introduction** **Kevin Zhang,** *Intel, Hillsboro, OR*
8:30	**Embedded Memories for Mobile Platforms Architectures** **Franck Seigneret,** *Texas Instruments, Nice, France*
9:30	**Embedded SRAM Design & Scaling Trend** **Hiroyuki Yamauchi,** *Fukuoka Institute of Technology, Fukuoka, Japan*
10:30	Break
10:45	**High-Performance eDRAM Design** **Harold Pilo,** *IBM, Essex Junction, VT*
11:45	**Embedded DRAM Technology for Consumer Electronics** **Hiroki Shirai,** *NEC, Kanagawa, Japan*
12:45	Lunch
1:45	**Embedded Flash Memory for MCU/SoC** **Masahiro Hatanaka,** *Renesas Technology, Hyogo Japan*
2:45	**Embedded MRAM Technology and Applications** **Tom Andre,** *Freescale, Austin, TX*
3:45	Break
4:00	**Embedded FeRAM Technology and Applications** **Shoichiro Kawashima,** *Fujitsu, Kawasaki, Japan*
5:00	**Summary/Conclusion** **Kevin Zhang,** *Intel, Hillsboro, OR*

F2: Wide-Dynamic-Range Imaging

Organizer: **Albert Theuwissen,** *Delft University of Technology, Delft, Netherlands/ Harvest Imaging, Bree, Belgium*

Committee: **Dan McGrath,** *Eastman Kodak, Rochester, NY*
Jed Hurwitz, *Gigle Semiconductors, Edinburgh, UK*
Hirofumi Sumi, *Sony, Tokyo, Japan*
Boyd Fowler, *Fairchild Imaging, Milpitas, CA*
Makato Ikeda, *University of Tokyo, Tokyo, Japan*
Takao Kuroda, *Matsushita, Kyoto, Japan*
Johannes Solhusvik, *Micron Technology, Oslo, Norway*
Yonghee Lee, *Samsung, Gyeonggi-Do, Korea*

If the silicon sensors/cameras are compared to the human eye, then in many aspects CCD and CMOS image sensors can perform better than the human visual system. Examples are image-capturing speed, radiation hardness, and the operating temperature. But the human eye outperforms silicon devices when it comes to power dissipation, image processing and dynamic range. The dynamic range of the human eye is about 90dB, while CCDs and CMOS imagers are about 72dB. The demand for solid-state image sensors that have a dynamic range far beyond the dynamic range of the human eye is growing rapidly. Application examples are medical, automotive, and machine vision. Even in consumer devices in which the pixels are shrinking, the requirements on dynamic range are increasing.

This forum is organized to contribute to a better understanding of the dynamic-range issues and to stimulate creativity in this field.

Forum Agenda:

Time	Topic
8:00	Breakfast
8:20	**Introduction** **Albert Theuwissen,** *Delft University of Technology, Delft, Netherlands/ Harvest Imaging, Bree, Belgium*
8:30	**Wide Dynamic Range : What Should I Care About?** **Bart Dierickx,** *Caeleste, Antwerp, Belgium*
9:20	**Other Limiting Factors** **Ricardo Motta,** *PIXIM, Mountain View, CA*
10:10	Break
10:30	**Wide Dynamic Range on Pixel Level** **Makoto Ikeda,** *University of Tokyo, Tokyo, Japan*
11:20	**Wide Dynamic Range on System Level** **Koichi Mizobuchi,** *Texas Instruments, Ibaraki, Japan*
12:10	Lunch
1:20	**Processing of High-Dynamic-Range Images** **Eric Reinhard,** *University of Bristol, Bristol, UK*
2:10	**Applications: What Do They Care About?** **Myung Ho Yoo,** *Samsung, Gyeonggi-Do, Korea*
3:00	Break
3:20	**Automotive Applications** **Dirk Hertal,** *Sensata, Cambridge, MA*
4:10	Panel Discussion
5:00	Conclusion

F3: Architectures and Circuit Techniques for Nanoscale RF CMOS

Co-Organizers: **Stefan Heinen,** *Infineon Technologies, Duisburg, Germany*
Francesco Svelto, *University of Pavia, Pavia, Italy*

Committee: **Jan Craninckx,** *IMEC, Leuven, Belgium*
Mototsugu Hamada, *Toshiba, Kawasaki,Japan*
Domine Leenaerts, *NXP, Eindhoven, Netherlands*
Chris Rudell, *Intel, Santa Clara, CA*

RF CMOS has become a mature technology over the last decade. RF SoC realizations of wireless systems are standard today for connectivity purposes, where first attempts are made to integrate even the PA amplifier for WLAN or DECT. The volume requirements of low-cost GSM/GPRS/EDGE mobile phones are driving these SoCs from 0.13µm to nanoscale technology nodes. 3G and 4G systems require the use of the 45nm or even 32nm node to cope with the power and cost targets. The high f_t of nanoscale CMOS is a key enabler for the use of RF CMOS in millimeter wave systems for data transmission or radar applications.

CMOS technologies at 65nm and below are a challenge for RF and mixed-signal circuits techniques. This forum gives insight into the design requirements provided by leading industry experts. Any nanoscale design must cope with the low supply voltage while manufacturing and variability aspects have to be considered. The increasing performance of digital circuitry with respect to power and speed leads to new architectures based on the corresponding integration tradeoffs for analog, RF and digital functions.

The forum concludes with a panel discussion where the attendees have the opportunity to ask questions and to share their views. Attendance is limited and pre-registration is required. This all-day forum encourages open information exchange. The targeted participants are circuit designers and concept engineers working on wireless systems who want to learn about the impact of nanoscale technologies in circuit and system design.

Forum Agenda:

Time	Topic
8:00	Breakfast
8:15	**Introduction** **Stefan Heinen,** *Infineon Technologies, Duisburg, Germany*
8:45	**Analog and RF Performance Perspectives of (Sub-) 32nm CMOS** **Stefaan Decoutere,** *IMEC, Leuven, Belgium*
9:30	**Foundry Technologies for Nanoscale RF Integration** **Shine Chung,** *TSMC, Hsinchu, Taiwan*
10:15	Break
10:45	**Nanometer CMOS is a Statistical Challenge!** **Marcel Pelgrom,** *NXP, Eindhoven, Netherlands*
11:30	**RF SoC Architecture Trends and Requirements in Deep-Submicron CMOS: A Perspective** **Khurram Muhammad,** *Texas Instruments, Dallas, TX*
12:15	Lunch
1:15	**Low-Voltage Transceiver Design in 45nm CMOS with an Emphasis on WiMAX** **Chris Rudell,** *Intel, Santa Clara, CA*
2:00	**mmW Design in Nanoscale CMOS** **Didier Belot,** *ST Microelectronics, Crolles, France*
2:45	Break
3:15	**UWB Circuit Design in 90nm, 65nm, and 45nm CMOS** **Domine Leenaerts,** *NXP, Eindhoven, Netherlands*
4:00	**Circuit Design in 45nm CMOS Process** **Lukas Doerrer,** *Infineon Technologies, Villach, Austria*
4:45	Panel Discussion
5:15	Conclusion

SE1: Green Electronics: Environmental Impacts, Power, E-Waste

Organizer: **Jan Sevenhans,** *AMI Semiconductor, Vilvoorde, Belgium*

Chair: **Rudolf Koch,** *Infineon, Munich, Germany*

Electronics companies in automotive and industrial applications are creating the green electronic brains of industry. The electronic brains are needed in petrol combustion cars and hybrid cars to control combustion and power generation so as to reduce the petrol consumption gallons-per-mile and to eliminate pollution to near-zero-ppm carbon-dust-per-kilowatt. The next step for the electronics industry is to provide the technology for new electronic sensors needed for pollution monitoring and policing of the green laws in industrial areas worldwide, with United Nations supervision. The green electronics revolution needs to go worldwide to China and the Far East as well as to Europe, the US and all continents to save all creatures for generations to come. Engineers will provide the electronics needed to address the challenges facing us in making a greener environment.

Time	Topics
7:30	**Green Fab and Manufacturing** ***Duane S. Boning***, *MIT, Cambridge, MA*
7:45	**Green Packaging** ***Gary Hamming***, *Amkor Technology, Chandler, AZ*
8:00	**Automotive Green Electronics** ***Marcos Laraia***, *AMI Semiconductor, Pocatello, ID*
8:15	**Green Aspects of Photovoltaic Cell Processing and its Applications** ***Robert Mertens***, *IMEC, Leuven, Belgium*
8:30	**Green Hybrid Car Electronics** ***Justin Ward***, *Toyota, Gardena, CA*
8:45	**Environmental Push for Green** ***Martin Hojsik***, *Greenpeace International, Bratislava, Slovak Republic*
9:00	Panel Discussion

SE2: MEMS for Frequency Synthesis and Wireless RF Communications (or Life without Quartz Crystal)

Organizer: **Christian Enz,** *CSEM, Neuchâtel, Switzerland*

Chair: **Ernesto Perea,** *STMicroelectronics, Crolles, France*

Many recent start-ups are now proposing silicon MEMS resonators as a replacement of quartz resonators for basic frequency and time reference, which are a crucial component in almost every electronic system. This Evening Session overviews the recent developments in Si MEMS resonators for time and frequency references. It will present technological and electronic solutions for implementing a highly stable and accurate temperature-compensated frequency reference for frequency synthesis modules covering a wide range of frequencies. It will also address the many challenges such as stability, phase noise, and packaging and will look at the perspective of integrating the MEMS devices with other passives such as BAW resonators and ultimately with the radio chip in a SiP. Four top experts in the field will give different perspectives and discuss the many challenges remaining to achieve the future “life without quartz crystals”.

Time	Topic
7:30	**Silicon Resonators for Ultra-Compact High-Performance Timing References** **Bernhard Boser,** *SiTime, Sunnyvale, CA*
8:00	**Micromechanical Circuits for Communications-Grade Frequency Control** **Clark Nguyen,** *University of California, Berkeley, CA*
8:30	**Integrating Si-MEMS, BAW Resonators and RF-CMOS in a SiP for Ultra Low Power Radio** **Jacek Baborowski,** *CSEM, Neuchâtel, Switzerland*
9:00	**RF MEMS for Reconfigurable Radio** **Kazuya Masu,** *Tokyo Institute of Technology, Yokohama, Japan*

PLENARY SESSION - INVITED PAPERS

Chair: **Timothy Tredwell**, *Carestream Health, Rochester, NY*
ISSCC Executive-Committee Chair

Associate Chair: **Yoshiaki Hagihara**, *Sony, Atsugi, Japan*
ISSCC Program-Committee Chair

FORMAL OPENING OF THE CONFERENCE **8:15AM**

1.1 The 2nd Wave of Digital Consumer Revolution: Challenges and Opportunities **8:30AM**

Hyung Kyu Lim, *CEO, Samsung Advanced Institute of Technology, Yongin-si, Korea*

Consumer devices are being interconnected through the Internet, bringing in unparalleled increase of productivity and quality of life, as well as profound changes in life style.

The semiconductor technology faithfully obeyed Moore's law enabling high performance, miniaturization, and cost reduction. It also led many technological innovations in computing, communications and storage device areas. Innovations in digital signal processing have enabled real-time multimedia entertainment through high-speed broadband access. Internet became a novel platform for new breeds of online social networks and communities creating innovative value-adds. Technological advancement in high-resolution flat panel displays, and advanced audio/video signal processing produced more vivid audio and video for the consumer entertainment. Such succession of innovations has empowered consumer devices with high performance and various functionalities. The advancement of mass production capability further enabled commoditization and proliferation of consumer devices for the masses.

Such 1st waves of digital consumer revolution drove the dramatic improvement in our quality of life through technology innovations. As the commoditization further progresses and the penetration rate grows, however, consumers are demanding sophisticated products and services to express their unique personality and life style beyond basic needs. Such consumer needs for new life style will be the main driver for new consumer devices and related technological innovations, leading to a 2nd wave of the digital consumer revolution.

In the 2nd wave of the digital consumer revolution, consumer needs will drive the innovation of new services and devices, **true mobile internet** and **next digital home**. They will also require new technological innovations, especially in the areas of mobile Internet devices and advanced IPTV. Mobile devices will be transformed into a personal agent through mobile Internet and highly advanced user interfaces. Advanced IPTV will become a hub in the digital home, providing an exciting experience with a variety of content. In order to help realize such human-centric vision of true quality of life and style, continuous innovations are required in the field of computing, communications and displays where semiconductor technology lies at the core.

1.2 Surface and Tangible Computing, and the "Small" Matter of People and Design **9:10AM**

Bill Buxton, *Principal Researcher, Microsoft Research, Toronto, Ontario / Redmond, Washington*

Developments in electronic technologies, integration, and fabrication have made way for products and services that were restricted to the domain of science fiction only a few years ago. In one direction, this has led to small powerful mobile devices that make Dick Tracy's watch look quaint rather than radical. In the other direction, we now clearly see the day when the living-room is wall-papered with a 100dpi display that rivals the experience previously available only in the cinema. But the real significance of change is not in any individual gadget, itself – regardless of scale – but in the inter-relationship with other gadgets of its kind.

So, while it is undoubtedly true that, "To reap the promised rewards, design and system integration must master all levels of the technology jigsaw puzzle", it is equally true that such mastery must take into account what constitutes the relevant levels, technologies, and requisite skills. To the extent that any complex system, structure or organism is a technology, yes, we can view things in technological terms. But whatever the language, "mastery", in any meaningful sense will only come through the larger holistic perspective – one that realizes (and takes into full account) that it is not the device or object that people ultimately value, but, rather, the experience and services that it engenders.

In this presentation, we look at the evolution of two different classes of computational device: first, large surface-type computational devices – such as digital table-tops; and, second, small graspable computational objects – such as mobile phones and MP3 players. We show how these two extremes of the computational spectrum can meet in a seamless integrated experience, and discuss some of the implications of our view of fruitful paths for future circuit design.

ISSCC, SSCS, JSSCC, & IEEE AWARD PRESENTATIONS **9:50AM**

BREAK **10:20AM**

1.3 Embedded Processing at the Heart of Life and Style **10:35AM**

Mike Muller, *CTO, ARM, Cambridge, UK*

From pacemakers to mobile phones to passenger jets, most people interact with electronic devices powered by embedded processor cores every day without a second thought. This penetration into everyday lives across such a broad range of applications requires the embedded core developer to work in close partnership with many of the world's leading semiconductor companies and OEMs, demanding close attention to technology trends from fundamental technology up to application requirements.

In the trade off between performance, power and die area, there is no right answer as each application has its own requirements. A diagnostic device that passes through the intestines may require 7-to-10 hours of battery life, while a pacemaker may require years; power consumption for an airbag deployment circuit on the other hand is not so critical, but failure free performance is literally life saving.

There is an insatiable appetite for computing power in efficiency-constrained environments. Silicon technology scaling has stopped delivering these improvements for free as a side effect of density scaling, which is driving the industry towards deeper application understanding and domain specific architectures. The IP business model facilitates this evolution as it frees resources to allow differentiation of solutions while preserving a common DNA between implementations. This business model results in orders-of-magnitude reduction of development costs for the industry and allows it to extend scaling well into the next decade. However, solutions will increasingly need to cut across circuit, architecture, and software boundaries to deliver efficient and scalable solutions for future generations.

1.4 Why Can't A Computer Be More Like A Brain? Or What To Do With All Those Transistors? **11:15AM**

Jeff Hawkins, *Founder, Numenta, Menlo Park, CA*

Why is it so difficult for computers to perform tasks that humans do quickly and easily? For over fifty years we have tried to program computers to recognize images, understand language, control robots, and learn on their own. Although we have had some limited successes, what is more remarkable is how little progress we have made. Large increases in memory capacity and CPU performance have not resulted in corresponding improvements in performance on AI tasks. Machine intelligence is in need of new approaches.

"Hierarchical Temporal Memory" (HTM) explains the behavior of the human neocortex, and provides a framework for building models that can be executed on conventional computers. The broad and flexible capabilities enabled by HTM may be an effective means of dramatically advancing artificial intelligence hosted in high-performance computer platforms. Research suggests that the structure of the neocortex is hierarchical, and that the emulation of 6 levels of hierarchy is sufficient to achieve sophisticated recognition and analysis of visual images. Presently, HTM technology is being explored in existing computer architectures; the age of intelligent machines may be just beginning, and if so, there will be many opportunities to rethink how integrated circuits may play a leading role.

Conclusion **11:55AM**

IMAGE SENSORS & TECHNOLOGY

Chair: Yong-Hee Lee, Samsung Electronics, Gyeonggi-do, Korea
Associate Chair: Jed Hurwitz, Gigle Semiconductor, Edinburgh, Scotland

2.1 A 128×128 Single-Photon Imager with on-Chip Column-Level 10b Time-to-Digital Converter Array Capable of 97ps Resolution

1:30 PM

C. Niclass, C. Favi, T. Kluter, M. Gersbach, E. Charbon
EPFL, Lausanne, Switzerland

A highly integrated CMOS image sensor for time-resolved optical sensing is designed for use in 3D imaging, optical range finding, fluorescence lifetime imaging, imaging extremely fast phenomena and imaging based on time-correlated single-photon counting. The sensor comprises an array of 128×128 single-photon avalanche photo-diode pixels, a band of 32 time-to-digital converters and a 7.68Gb/s readout system. The imager is capable of a 97ps typical time resolution within a 100ns range.

2.2 A 5000S/s Single-Chip Smart Eye-Tracking Sensor

2:00 PM

D. Kim, J. Cho, S. Lim, D. Lee, G. Han
Yonsei University, Seoul, Korea

An eye-tracking sensor system generates a two-dimensional coordinate of the point at which the user is looking. It can be used as a human interface device for a number of applications. The single-chip eye tracker includes pixel-level analog and digital signal processing including glint removal. Test results confirm a coordinate accuracy of $\pm\sqrt{2}$pixels at 5000S/s. The chip consumes 100mW from a 3.3V supply and occupies 7.5mm^2.

2.3 A 3MPixel Multi-Aperture Image Sensor with 0.7µm Pixels in 0.11µm CMOS

2:30 PM

K. Fife, A. El Gamal, H-S. Wong
Stanford University, Stanford, CA

A multi-aperture imager sensor is designed to reduce lens requirements, produce 3D maps and improve pixel-defect tolerance. It comprises a 166×76 array of 16×16 0.7µm full-frame transfer CCD sub-arrays, a CMOS readout circuit and per-column 10b ADCs fabricated in a 0.11µm CMOS process. Snap-shot image acquisition with CDS is performed at up to 15fps. The array has 0.15V/lx·s sensitivity, 3500e$^-$ full-well capacity, 5e$^-$ read noise, 25e$^-$/s dark signal, 57dB DR and 35dB peak SNR.

Break 3:00 PM

2.4 A 140dB-Dynamic-Range MOS Image Sensor with In-Pixel Multiple-Exposure Synthesis

3:15 PM

T. Yamada, S. Kasuga, T. Murata, Y. Kato
Matsushita Electric Industrial, Takatsuki, Japan

A wide dynamic range 177×144pixel CMOS image sensor that can simultaneously capture both dark and bright objects in one synthesized frame has an analog accumulator within each 8µm pixel to synthesize a wide dynamic range image from multiple exposures. The sensor is capable of acquiring a 140dB dynamic range image at 15fps without external frame buffers.

2.5 A White-RGB CFA-Patterned CMOS Image Sensor with Wide Dynamic Range

3:30 PM

E. Yoshitaka
Toshiba, Yokohama, Japan

A 2Mpixel CIS for mobile imaging applications has a pixel pitch of 2.2µm and is fabricated in a 0.13µm CMOS technology. The sensor uses a white-RGB color filter array instead of the regular Bayer pattern to improve the low-light SNR by about 3dB. The array also achieves a wide dynamic range by using charge skimming and multiple acquisitions. The dynamic range can be expanded by 8 while maintaining the improved SNR.

2.6 A 3.6pW/frame-pixel 1.35V PWM CMOS Imager with Dynamic Pixel Readout and no Static Bias Current

3:45 PM

K. Kagawa, S. Shishido, M. Nunoshita, J. Ohta
Nara Institute of Science and Technology, Ikoma, Japan

A 0.42µW 128×96 pixel CIS fabricated in a 0.35µm technology with 10µm pixels employs pixel-level amplitude-to-pulse-width conversion and dynamic pixel readout using a modified 3T pixel. The power is more than 30× less than that dissipated with static readout. Dynamic pixel readout reduces power dissipation and simultaneously improves sensor performance.

2.7 A CMOS Image Sensor Integrating Column-Parallel Cyclic ADCs with On-Chip Digital Error-Correction Circuits

4:15 PM

S. Kawahito[1], J-H. Park[2], K. Isobe[2], S. Suhaidi[1], T. Iida[1], T. Mizota[3]
[1]Shizuoka University, Hamamatsu, Japan, [2]Brookman Lab, Hamamatsu, Japan
[3]Sanei Hytechs, Hamamatsu, Japan

A 0.18µm CIS with column-parallel cyclic ADCs and on-chip digital error-correction circuits is presented. The columns are located on the upper and lower sides of the 7.5µm-pitch VGA image array. The digital error-correction circuits compensate for the effects of capacitor mismatch, finite amplifier gain and offset errors of the ADC, and increase the linearity to <0.05% (INL +7.2/-3.2LSB). The column ADC achieves 14b resolution (DNL +0.35/-0.98LSB) and 12b accuracy with a random noise floor of 250µV_{rms}.

2.8 A 2Mpixel 1/4-inch CMOS Image Sensor with Enhanced Pixel Architecture for Camera-Phones and PC Cameras

4:30 PM

J. Moholt[1], T. Willassen[1], J. Ladd[2], X. Fan[2], D. Gans[2]
[1]Micron, Oslo, Norway, [2]Micron, Boise, ID

A 2Mpixel 1/4-inch CIS with a 2.2µm pixel pitch uses a 2.5T shared-pixel structure with a column-activated diode reset structure that delivers high image quality and increased sensitivity. The sensor complies with the standard mobile imaging architecture. It operates between -30°C and +70°C, and has a supply range of 2.4 to 3.1V. When operating at full resolution at 30fps the sensor consumes 200mW, while in standby mode it draws 1µA.

2.9 Low-Crosstalk and Low-Dark-Current CMOS Image-Sensor Technology Using a Hole-Based Detector

4:45 PM

E. Stevens[1], H. Komori[2], H. Doan[1], H. Fujita[1], J. Kyan[1], C. Parks[1], G. Shi[1], J. Wu[1]
[1]Eastman Kodak, Rochester, NY, [2]Eastman Kodak, Yokohama, Japan

A CIS with a hole-based pinned photodiode is presented. The detector reduces crosstalk by 3× and dark current up to 5× compared with an equivalent electron-based pinned photodiode detector. This technology is capable of full-well capacities of 60kh, 11kh and 4kh for 4.3µm, 1.75µm and 1.4µm pixels, respectively. A red-into-green pixel crosstalk of 7% is achieved at 650nm for a 4.3µm pixel, and the measured dark-current density is 25pA/cm^2 at 60°C.

2.10 A CMOS Image Sensor with a Buried-Channel Source Follower

5:00 PM

X. Wang[1], M. Snoeij[1,2], P. Rao[1], A. Mierop[3], A. Theuwissen[1,4]
[1]Delft University of Technology, Delft, Netherlands, [2]Texas Instruments, Erlangen, Germany,
[3]DALSA Semiconductor, Eindhoven, Netherlands, [4]Harvest Imaging, Bree, Belgium

A CIS fabricated in a 0.18µm process with a 4T pinned-photodiode pixel and a buried-channel source follower (BSF) is presented. Measurements confirm that the BSF reduces the dark random noise by more than 50% and improves the output swing by almost 100% when compared with a surface-channel NMOS source follower. Moreover, the BSF reduces the variance of the dark random noise distribution by minimizing the number of pixels that have RTS noise.

Conclusion **5:15 PM**

FILTERS AND AMPLIFIERS

Chair: JoAnn Close, Analog Devices, San Jose, CA
Associate Chair: Vadim Gutnik, Impinj, Newport Beach, CA

3.1 A Widely-Tunable Reconfigurable CMOS Analog Baseband IC for Software-Defined Radio

1:30 PM

M. Kitsunezuka, S. Hori, T. Maeda
NEC, Kawasaki, Japan

A reconfigurable CMOS analog baseband IC based on a widely tunable discrete-time filter provides Butterworth, Chebyshev and Elliptic responses with bandwidths between 400kHz and 12MHz. The chip is fabricated in a 90nm CMOS process, consumes 5mA, has a P_{-1dB} of +9dBm with a 1V supply, an input-referred integrated in-band noise of $470\mu V_{rms}$ and a die area of $0.57mm^2$.

3.2 A Gain-Boosted Discrete-Time Charge-Domain FIR LPF with Double-Complementary MOS Parametric Amplifiers

2:00 PM

A. Yoshizawa, S. Iida
Sony, Tokyo, Japan

Double-complementary MOS parametric amplifiers are implemented to boost the gain of a discrete-time charge-domain FIR LPF. Step-variable gain is achieved through activating and deactivating the parametric amplifiers. The filter gain increases by 20dB when boosted and the clock generator current increases 2.3mA.

3.3 A Continuous-Time Hexagonal Field-Programmable Analog Array in 0.13µm CMOS with 186MHz GBW

2:30 PM

J. Becker, F. Henrici, S. Trendelenburg, M. Ortmanns, Y. Manoli
University of Freiburg, IMTEK, Freiburg, Germany

A field-programmable analog array for reconfigurable instantiations of continuous-time analog filters is presented. The circuit is realized in a 0.13µm CMOS technology and contains 55 digitally-tunable G_m-cells connected in a unique hexagonal topology without switches in the signal-path. It achieves a maximum GBW of 186MHz in simulations and measurements with a total power dissipation of 70mW.

Break 3:00 PM

3.4 A 6th-Order 100µA 280MHz Source-Follower-Based Single-Loop Continuous-Time Filter

3:15 PM

S. D'Amico, M. De Matteis, A. Baschirotto
University of Salento, Lecce, Italy

A single-loop filter architecture based on positive- and negative-impedance voltage followers yields a drastic reduction in power consumption with respect to the state of the art. The architecture is demonstrated by a filter for ultra wide-band receivers implemented in 0.13µm CMOS. The 6^{th}-order filter has a 280MHz cut-off frequency, an 11dBm IIP3, -140dBm input-referred noise and draws 100µA from a 1.2V supply.

3.5 A Current-Feedback Instrumentation Amplifier with 5µV Offset for Bidirectional High-Side Current-Sensing

3:45 PM

J. Witte, J. Huijsing, K. Makinwa
Delft University of Technology, Delft, Netherlands

An instrumentation amplifier for bidirectional high-side current-sensing applications uses an indirect current-feedback topology to achieve a CMRR of 140dB and a CM input voltage range from 1.9 to 30V. Chopping and auto-zeroing are used to achieve an offset voltage of less than 5µV. Trimmed gain-setting resistors yield 0.1% accuracy. The circuit is fabricated in a 0.8µm BiCMOS process with HV transistors and laser-trimmed thin-film resistors and occupies 2.5mm^2.

3.6 A BiCMOS Operational Amplifier Achieving 0.33µV/°C Offset Drift using Room-Temperature Trimming

4:15 PM

M. Bolatkale[1], M. Pertijs[2], W. Kindt[2], J. Huijsing[1], K. Makinwa[1]
[1]Delft University of Technology, Delft, Netherlands
[2]National Semiconductor, Delft, Netherlands

A MOS-input operational amplifier has a reconfigurable input stage that enables extraction of temperature-dependent offset components from room-temperature measurements. The opamp is fabricated in a 0.5µm BiCMOS process and measures 1.4mm^2. After room-temperature trimming, it achieves an offset of ±45µV (±3σ) and an offset drift of ±0.33µV/°C (±3σ). The operational amplifier dissipates 5.5mW from a 5V supply.

3.7 130dB-DR Transimpedance Amplifier with Monotonic Logarithmic Compression and a High-Current Monitor

4:30 PM

D. Micusik, H. Zimmermann
TU Vienna, Vienna, Austria

A 0.35µm SiGe BiCMOS transimpedance amplifier (TIA) with 200mA input-current overdrive is described. This TIA is linear for small input currents, while large input currents are logarithmically compressed in two stages to avoid saturating the TIA. The -3dB BW is 250MHz and the equivalent RMS input noise current for this BW is 58nA with 2pF photodiode capacitance.

Conclusion **4:45 PM**

MICROPROCESSORS

Chair: Don Draper, Rambus, Los Altos, CA
Associate Chair: Sonia Leon, Sun Microsystems, Santa Clara, CA

4.1 A Third-Generation 65nm 16-Core 32-Thread Plus 32-Scout-Thread CMT SPARC® Processor

1:30 PM

M. Tremblay, S. Chaudhry
Sun Microsystems, Santa Clara, CA

A 2.3GHz 396mm^2 16-core 32-thread processor with deep out-of-order retirement and transactional memory is fabricated in 65nm CMOS. The logical and physical design of this high-end microprocessor enable high throughput, high single-thread performance, mainframe-class reliability, availability and serviceability (RAS), hardware transactional memory, and linear scalability.

4.2 Implementation of a Third-Generation 16-Core 32-Thread CMT SPARC® Processor

2:00 PM

G. Konstadinidis, M. Rashid, P. Lai, Y. Otaguro, Y. Orginos, S. Parampalli, M. Steigerwald, S. Gundala, R. Paypali, L. Rarick, I. Elkin, Y. Ge, I. Parulkar
Sun Microsystems, Santa Clara, CA

A 65nm third-generation chip-multithreading SPARC® processor operates at 2.3GHz and is targeted for high-performance servers. It is optimized for both single- and multi-threaded applications. Circuit innovations in memory arrays, register files, and floating-point hardware boost performance and circuit robustness with minimum area overhead.

4.3 Migration of Cell Broadband Engine™ from 65nm SOI to 45nm SOI

2:30 PM

O. Takahashi[1], C. Adams[2], E. Behnen[1], O. Chiang[1], S. Cottier[1], P. Coulman[1], J. Culp[3], G. Gervais[1], M. Gray[4], Y. Itaka[5], C. Johnson[2], F. Kono[5], L. Maurice[1], K. McCullen[4], L. Nguyen[1], Y. Nishino[6], H. Noro[5], J. Pille[7], M. Riley[1], S. Tokito[6], T. Wagner[3], H. Yoshihara[6]
[1]IBM, Austin, TX
[2]IBM, Rochester, MN
[3]IBM, Hopewell Junction, NY
[4]IBM, Essex Junction, VT
[5]Toshiba America Electronic Components, Austin, TX
[6]Sony Computer Entertainment of America, Austin, TX
[7]IBM, Boeblingen, Germany

We describe the challenges of migrating the Cell Broadband Engine™ design from 65nm SOI to 45nm SOI using mostly an automated approach. The cycle-by-cycle machine behavior is preserved. The focus areas are migration effectiveness, power reduction, area reduction, and DFM improvements. The chip power consumption is reduced roughly by 40% and the chip area is reduced by 34%.

Break 3:00 PM

4.4 TILE64™ Processor: A 64-Core SoC with Mesh Interconnect

3:15 PM

S. Bell, B. Edwards, J. Amann, R. Conlin, K. Joyce, V. Leung, J. MacKay, M. Reif
Tilera, Westborough, MA

An SoC with 64 tiles connected by mesh networks for networking and multimedia markets is fabricated in 90nm CMOS. Each tile consists of a processor with a 3-way VLIW execution pipeline, memory management, cache, and a switch to manage communication to and from five independent on-chip networks. The chip provides up to 384GOPS with 240GB/s of on-chip bisectional bandwidth.

4.5 An 8640MIPS SoC with Independent Power-Off Control of 8 CPUs and 8 RAMs by Automatic Parallelizing Compiler

3:45 PM

M. Ito[1], T. Hattori[1], Y. Yoshida[1], K. Hayase[1], T. Hayashi[1], O. Nishii[1], Y. Yasu[1], A. Hasegawa[1], M. Ito[2], H. Mizuno[2], K. Uchiyama[2], T. Odaka[2], J. Shirako[3], M. Mase[3], K. Kimura[3], H. Kasahara[3]
[1]Renesas Technology, Tokyo, Japan
[2]Hitachi, Tokyo, Japan
[3]Waseda University, Tokyo, Japan

A 104.8mm^2 90nm CMOS 600MHz SoC integrates 8 processor cores and 8 user RAMs in 17 separate power domains and delivers 33.6GFLOPS. An automatic parallelizing compiler assigns tasks to each CPU and controls its power mode including power supply in accordance with its processing load and status. The compiler also uses barrier registers to achieve fast and accurate CPU synchronization.

4.6 A 65nm 2-Billion-Transistor Quad-Core Itanium® Processor

4:15 PM

B. Stackhouse
Intel, Fort Collins, CO

An Itanium® processor is implemented in 8M 65nm CMOS and measures 21.5×32.5mm^2. The processor has four dual-threaded cores, a system interface and 30MB of cache. Quickpath high-speed links enable peak processor-to-processor bandwidth of 96GB/s and peak memory bandwidth of 34GB/s.

4.7 Circuit Design for Voltage Scaling and SER Immunity on a Quad-Core Itanium® Processor

4:45 PM

D. Krueger[1], E. Francom[1], J. Langsdorf[2]
[1]Intel, Fort Collins, CO
[2]Intel, Hudson, MA

A 700mm^2 65nm Itanium® processor triples the logic circuitry of its predecessor. Voltage-frequency scaling to contain power consumption is improved by circuit changes that enable lower voltage operation. Furthermore, per-socket error rate is held constant with the use of SER-hardened latches and register files that reduce SER by 80 to 100× over unprotected structures.

Conclusion **5:15 PM**

HIGH-SPEED TRANSCEIVERS

Chair: Hui Pan, Broadcom, Irvine, CA

Associate Chair: Hong-June Park, Pohang University of Science and Technology, Pohang, Korea

5.1 An 8Gb/s Transceiver with a 3×-Oversampling 2-Threshold Eye-Tracking CDR Circuit for a -36.8dB-loss Backplane

1:30 PM

K. Fukuda[1], H. Yamashita[1], F. Yuki[1], M. Yagyu[1], R. Nemoto[1], T. Takemoto[1], N. Chujo[2], K. Yamamoto[2], H. Kanai[2], A. Hayashi[1]
[1]Hitachi, Tokyo, Japan
[2]Hitachi, Kanagawa, Japan

A 90nm CMOS 8Gb/s transceiver comprises a transmitter with a 5-tap FFE, a receiver with an analog equalizer, a 2-tap DFE and a 2-threshold eye-tracking CDR. The transceiver achieves a BER of $<10^{-12}$ when operating over a 160cm backplane channel with -36.8dB of loss at 4GHz. The TX and RX together consume 232mW and occupy 0.286mm^2.

5.2 A 40Gb/s CMOS Serial-Link Receiver with Adaptive Equalization and CDR

2:00 PM

C-F. Liao, S-I. Liu
National Taiwan University, Taipei, Taiwan

A 40Gb/s serial-link receiver incorporates an adaptive single-loop parallel-path equalizer and a full-rate CDR circuit. A 5-latch bang-bang phase detector is proposed in the CDR circuit to enhance the speed and reduce the power dissipation. Fabricated in 90nm CMOS, the receiver reproduces the data with 500mV$_{pp}$ output swing and 9.6ps$_{pp}$ jitter with BER$<10^{-12}$ while consuming 115mW. The chip occupies 0.77×0.7mm^2 including the pads.

5.3 A 20Gb/s Duobinary Transceiver in 90nm CMOS

2:30 PM

J. Lee, M-S. Chen, H-D. Wang
National Taiwan University, Taipei, Taiwan

A fully integrated 20Gb/s duobinary transceiver implemented in a 90nm CMOS process is presented. The circuit incorporates a skew-tolerance precoder and a 3-tap FFE in the transmitter, and an adaptive decoder in the receiver. It achieves error-free operation with 2^{31}-1 PRBS data over 40cm Rogers and 10cm FR4 channels.

Break 3:00 PM

5.4 A 6Gb/s RX Equalizer Adapted Using Direct Measurement of the Equalizer Output Amplitude

3:15 PM

H. Uchiki, Y. Ota, M. Tani, Y. Hayakawa, K. Asahina
Renesas Technology, Itami, Japan

An adaptive equalization scheme uses a 2-step direct amplitude measurement. Jitter at the output of the adaptive equalizer is reduced to 50ps for 6Gb/s operation over a 15-inch FR4 backplane. The RX equalizer and the adaptation logic consume 10.9mW and 2.4mW, respectively. The chip occupies 170×320μm^2 in 90nm CMOS.

5.5 A 10Gb/s IEEE 802.3an-Compliant Ethernet Transceiver for 100m UTP Cable in 0.13µm CMOS

3:45 PM

S. Gupta, S. Kasturia, J. Tellado, S. Begur, F. Yang, V. Balan, M. Inerfield, D. Dabiri, J. Dring, S. Goel, K. Muthukumarswamy, F. McCarthy, G. Golden, J. Wu, S. Arno
Teranetics, Santa Clara, CA

A transceiver for the IEEE 802.3an Ethernet standard implemented in 0.13µm CMOS consists of a 4-lane AFE running at 800MS/s and a digital processor in a 25×25mm^2 BGA package. Power consumption is 10.5W when the transceiver is transmitting and receiving at 10Gb/s over 100m of UTP cable. The transceiver supports interoperation with 100Mb/s and 1Gb/s Ethernet transceivers. The AFE occupies 55mm^2 and the digital processor occupies 150mm^2.

5.6 A Serial Data Transmitter for Multiple 10Gb/s Communication Standards in 0.13µm CMOS

4:15 PM

A. Lin, M. Loinaz
Aeluros, Mountain View, CA

A serial transmitter is designed for multiple 10Gb/s communication standards. The circuit features a 3-tap FIR filter to comply with SFP+ and Ethernet backplane requirements. In addition, the transmitter can serve as a 100Ω VCSEL driver in 10Gb/s Ethernet optical-module applications. Designed in a 0.13µm CMOS process, the transmitter dissipates 165mW and occupies 0.6mm^2.

5.7 A T-Coil-Enhanced 8.5Gb/s High-Swing Source-Series-Terminated Transmitter in 65nm Bulk CMOS

4:45 PM

M. Kossel, C. Menolfi, J. Weiss, P. Buchmann, G. von Bueren, L. Rodoni, T. Morf, T. Toifl, M. Schmatz
IBM Research, Rueschlikon, Switzerland

Implemented in 65nm bulk CMOS, the 8.5Gb/s transmitter exhibits an eye height exceeding 1.0V and has a return loss of <-16dB up to 10GHz owing to the use of 40×40µm^2 T-coils that are applied to the 1.5V-operated thick-oxide output slices. The equalization consists of a 5b 2-tap FIR filter whose adaptation is orthogonal to that of the impedance tuning. A duty-cycle restoration capability of 5× is achieved. The chip consumes 96mW at 8.5Gb/s and occupies 180×360µm^2.

5.8 A 3.2Gb/s 8b Single-Ended Integrating DFE RX for 2-Drop DRAM Interface with Internal Reference Voltage and Digital Calibration

5:00 PM

H-J. Chi[1], J-S. Lee[1], S-H. Jeon[1], S-J. Bae[2], J-Y. Sim[1], H-J. Park[1]
[1]Pohang University of Science and Technology, Pohang, Korea
[2]Samsung Electronics, Hwasung, Korea

A 3.2Gb/s/pin 8b 2-drop single-ended integrating DFE receiver is implemented in a 0.18µm CMOS process. The reference voltage is generated internally to reduce the external noise. A single-loop implementation of the LMS algorithm is used to decide the equalization coefficient. An open-loop DCC, embedded inside the PLL loop, makes the duty cycle of the PLL output 50±1%. The RX consumes 68mW and occupies 600×300µm^2. The PLL consumes 31mW and occupies 290×117µm^2.

Conclusion **5:15 PM**

UWB POTPOURI

Chair: Mark Ingels, IMEC, Leuven, Belgium
Associate Chair: Domine Leenaerts, NXP Semiconductors, Eindhoven, Netherlands

6.1 A 1.8Gpulse/s UWB Transmitter in 90nm CMOS

1:30 PM

M. Demirkan, R. Spencer
University of California, Davis, CA

A 1.8Gpulse/s FCC-compliant UWB transmitter comprises an FIR pulse generator and a PLL frequency synthesizer. The transmitter supports simultaneous PPM and BPSK modulation while achieving 1.9ps_{rms} and 15.1ps_{pp} jitter. Implemented in standard digital 90nm CMOS, the 2.83mm^2 transmitter consumes 227mW from a 1V supply.

6.2 A 0.18µm CMOS 802.15.4a UWB Transceiver for Communication and Localization

2:00 PM

Y. Zheng, M. Asaru, K-W. Wong, Y. The, A. Poh, D. Tran, W. Yeoh, D-L. Kwong
Institute of Microelectronics, Singapore, Singapore

An 802.15.4a compliant UWB transceiver chip operating from 3.1 to 9GHz over 12 channels is presented. The TRX allows coherent BPM-BPSK communication and precise ranging/localization. Realized in 0.18µm CMOS, the RX achieves an NF of 8.2 to 9.4dB, an IIP3 of -12 to -8dBm, and a sensitivity of -75 to -70dBm. At a peak-pulse transmission rate of 1Gb/s, 0.74nJ/b and 6.5nJ/b are consumed for TX and RX, respectively. A ranging accuracy of 3cm is achieved.

6.3 A CMOS UWB Camera with 7×7 Simultaneous Active Pixels

2:30 PM

T-S. Chu, H. Hashemi
University of Southern California, Los Angeles, CA

An UWB imaging camera with 2×2 antennas and 7×7 simultaneous active pixels is implemented in 0.13µm CMOS. The design consists of a 2D multi-beam architecture and a detector array. The 2D multi-beam array achieves a worst-case NF of 5.8dB, true time delay resolution of 17.5ps, and array gain of 24dB from 1 to 15GHz. With 3cm antenna spacing, this 2D camera achieves a 10° spatial resolution and ±30° of spatial coverage in each direction.

Break 3:00 PM

6.4 A Fully-Integrated 14-Band 3.1-to-10.6GHz 0.13µm SiGe BiCMOS UWB RF Transceiver

3:15 PM

O. Werther, M. Cavin, A. Schneider, R. Renninger, B. Liang, L. Bu, Y. Jin, J. Marcincavage
Alereon, Austin, TX

A fully integrated WiMedia-compliant UWB transceiver supporting band groups 1 to 6 (3.168 to 10.560GHz) is implemented in 0.13µm SiGe BiCMOS. The transceiver is packaged in a small 40-pin 5×5mm^2 micro-lead-frame (MLF) package and includes a broadband T/R switch, RF balun, and all PLL loop filter components. The receiver has an NF of 4.5dB and a dynamic range of more than 50dB. The transmitter meets US and international transmit mask requirements.

6.5 UWB Fast-Hopping Frequency Generation Based on Sub-Harmonic Injection Locking

3:45 PM

S. Dal Toso[1], A. Bevilacqua[1], M. Tiebout[2], S. Marsil[2], C. Sandner[2], A. Gerosa[1], A. Neviani[1]
[1]University of Padova, Padova, Italy
[2]Infineon, Villach, Austria

Sub-harmonic injection locking is used to generate fast-hopping carriers required in UWB for WiMedia systems. A 90nm CMOS prototype synthesizes the frequencies of band group 6 with a hop time shorter than 4ns. It occupies 0.074mm^2 and draws 30mA from a 1.2V supply. Phase noise at 8.71GHz is -112dBc (at 1MHz offset).

6.6 A 3-to-10GHz 14-Band CMOS Frequency Synthesizer with Spurs Reduction for MB-OFDM UWB Systems

4:00 PM

T-Y. Lu, W-Z. Chen
National Chiao-Tung University, Hsinchu, Taiwan

A 3-to-10GHz 14-band CMOS frequency synthesizer with spur reduction for MB-OFDM UWB systems is presented. Based on a single PLL and two-stage frequency mixing architecture, the image spurs are suppressed below -45dBc and improved by more than 22dB using an I/Q calibration for the single-side-band mixers. Implemented in 0.18µm CMOS, the chip draws 65mA from a single 1.8V supply.

6.7 A 0.6-to-10GHz Receiver Front-End in 45nm CMOS

4:15 PM

R. van de Beek, J. Bergervoet, H. Kundur, D. Leenaerts, G. van der Weide
NXP Semiconductors, Eindhoven, Netherlands

A 0.6-to-10GHz receiver front-end is realized in a baseline 45nm CMOS. The receiver has a broadband gain of 14dB and an NF of 7dB between 0.6 and 10GHz. The measured IIP3 of the total chain is slightly above 0dBm and the IIP2 is above 20dBm over the band of interest. Power dissipation is 90mW from a 1.2V supply.

6.8 A 90nm CMOS 60GHz Radio

4:30 PM

S. Pinel, S. Sarkar, P. Sen, B. Perumana, D. Yeh, D. Dawn, J. Laskar
Georgia Institute of Technology, Atlanta, GA

A 60GHz transmitter and a 60GHz receiver are integrated in standard 90nm CMOS. The super-heterodyne architecture supports the complete 57-to-66GHz bandwidth and enables data throughput exceeding 7Gb/s QPSK and 15Gb/s 16QAM when combined with a high-speed digital signal processor. The total DC power budget is below 200mW.

6.9 A 60kb/s-to-10Mb/s 0.37nJ/b Adaptive-Frequency-Hopping Transceiver for Body-Area Network

5:00 PM

N. Cho, J. Lee, L. Yan, J. Bae, H-J. Yoo
KAIST, Daejeon, Korea

A 60kb/s-to-10Mb/s body-channel transceiver for multimedia and health-care body-area network applications is designed and tested. To reject in-band interferences due to the human-body-antenna effect, adaptive frequency hopping is utilized. For 10Mb/s FSK and 4µs hopping time, a direct-switching modulator and a DLL-based demodulator are developed. The 0.18µm CMOS transceiver withstands -28dB SIR and consumes 0.37nJ/b.

Conclusion **5:30 PM**

TD: ELECTRONICS FOR LIFE SCIENCES
Chair: Chris Van Hoof, IMEC, Leuven, Belgium
Associate Chair: Satoshi Shigematsu, NTT, Atsugi, Japan

7.1 Life Thermoscope: Integrated Microelectronics for Visualizing Hidden Life Rhythm

1:30 PM

K. Yano, N. Sato, Y. Wakisaka, S. Tsuji, N. Ohkubo, M. Hayakawa, N. Moriwaki
Hitachi, Kokubunji, Japan

A 30cm^3 integrated module with 3-year battery life and total average system power of 5μA creates a wearable Sensornet/Internet terminal, integrating sensing, computing, wireless 802.15.4 transceiver, a battery, a display, a speaker and 3-button user interface. Based on innovations of human-activity sensing through temporal temperature rhythm extraction, a life rhythm image is constructed covering a four-month period.

7.2 A 1V Micropower System-on-Chip for Vital-Sign Monitoring in Wireless Body Sensor Networks

2:00 PM

A. Wong[1], D. McDonagh[1], G. Kathiresan[1], O. Omeni[1], O. El-Jamaly[1], T. Chan[2], P. Paddan[1], A. Burdett[1]
[1]Toumaz Technology, Abingdon, United Kingdom
[2]Future Waves, Abingdon, United Kingdom

An SoC for wireless body sensor networks integrates an ultra-low-power wireless ISM band transceiver, hardware MAC, microprocessor, I/O peripherals, memories, 10b $\Delta\sum$ ADC and custom sensor interfaces. The chip, implemented in 0.13μm CMOS and occupying 16mm^2, operates from supply voltages as low as 0.9V and is a disposable platform solution for "last meter" body area networks.

7.3 CMOS Mini Nuclear Magnetic-Resonance System and its Application for Biomolecular Sensing

2:30 PM

Y. Liu[1], N. Sun[1], H. Lee[2], R. Weissleder[2], D. Ham[1]
[1]Harvard University, Cambridge, MA
[2]Massachusetts General Hospital, Harvard Medical School, Boston, MA

A complete nuclear magnetic resonance (NMR) system occupying 2500cm^3 and weighing less than 2kg is made possible by integration of a highly sensitive and versatile RF transceiver including RF excitation pulse sequences in 0.18μm CMOS. The system's functionality is verified through proton NMR measurements in isotonic water and with biomolecular sensing. The system is 60× more sensitive, 40× smaller and 60× lighter than a commonly used state-of-the-art commercial benchtop NMR system. It can serve as a portable low-cost diagnostic system.

Break 3:00 PM

7.4 CMOS Imager Technologies for Biomedical Applications

3:15 PM

J. Burghartz, T. Engelhardt, H-G. Graf, C. Harendt, H. Richter, C. Scherjon, K. Warkentin
IMS CHIPS, Stuttgart, Germany

Two CMOS imager chips are described. The first is a sub-retinal implant, being the only imager chip ever implanted into a human eye that partially restores vision to a blind patient. The second is a miniature imager chip, based on a thin-film-on-CMOS (TFC) pixel technology provides an optimum trade-off between sensitivity and pixel size.

7.5 A 1600-pixel Subretinal Chip with DC-free Terminals and ±2V Supply Optimized for Long Lifetime and High Stimulation Efficiency

3:45 PM

A. Rothermel[1], V. Wieczorek[1], L. Liu[1], A. Stett[2], M. Gerhardt[2], A. Harscher[3]
[1]University of Ulm, Ulm, Germany
[2]NMI, Reutlingen, Germany
[3]Retina Implant, Reutlingen, Germany

A second-generation subretinal implant chip has low supply voltage and all DC-free terminals for long-life wired operation. Stimulation voltage is increased to $4V_{PP}$ with ±2V symmetrical supply by low voltage drop design. 40×40 pixel cells comprising light sensors and electrode drivers are addressed sequentially to improve power consumption and spatial resolution of perception. The 3×3.5mm^2 design is fabricated in a 0.35µm CMOS opto-technology.

7.6 A 128-Channel 6mW Wireless Neural Recording IC with On-the-Fly Spike Sorting and UWB Transmitter

4:15 PM

M. Chae[1], W. Liu[1,3], Z. Yang[1], T. Chen[1], J. Kim[1], M. Sivaprakasam[1], M. Yuce[2]
[1]University of California, Santa Cruz, CA
[2]University of Newcastle, Callaghan, Australia
[3]National Chiao-Tung University, Hsinchu, Taiwan

A fully integrated neural recording IC implements on-the-fly spike sorting and wireless telemetry for neural prostheses. Noise shaping eliminates frequent training thus enabling on-chip spike sorting. 90Mb/s UWB allows simultaneous 128 channel data transmission. The 8.8×7.2mm^2 0.35µm CMOS IC dissipates 6mW from a ±1.65V supply due to the sequential turn-on architecture.

7.7 A 256×256 CMOS Microelectrode Array for Extracellular Neural Stimulation of Acute Brain Slices

4:45 PM

N. Lei, K. Shepard, B. Watson, J. MacLean, R. Yuste
Columbia University, New York, NY

A 256×256 pixel microelectrode array capable of extracellular stimulation of acute brain slices is fabricated on a 4×4mm^2 die in 0.25µm CMOS. Each square electrode, 12.2µm in pitch, is capacitively coupled to the brain slice through a sheet of 20nm-thick hafnium oxide. Each electrode is capable of producing a unique stimulation pulse waveform with a timing resolution of 50ns and variable amplitude from 0.7V to 4.2V.

7.8 A 1.12mW Continuous Healthcare Monitor Chip Integrated on a Planar Fashionable Circuit Board

5:00 PM

H. Kim, Y. Kim, Y-S. Kwon, H-J. Yoo
KAIST, Daejeon, Korea

The planar fashionable circuit board (P-FCB) consisting of planar thin film technology on fabric and a direct chip integration technique are introduced to integrate chips and electronics with textiles directly. A 3×5mm^2 0.25µm CMOS Controller with a reduced transition read-out circuit consumes 1.12mW from a 2V supply at 1MHz. It is integrated with a planar humidity sensor and LEDs on P-FCB for continuous healthcare application.

Conclusion **5:15 PM**

SE3: From Silicon to Aether and Back

Co-Organizers: **Satoshi Tanaka,** *Renesas Technology, Komoro, Japan*
Marc Tiebout, *Infineon Technologies, Villach, Austria*

Chair: **Ali Hajimiri,** *California Institute of Technology, Pasadena,CA*

The interface from antenna to silicon IC is complicated by the proliferation of standards. Filtering, switching and interface to the antenna are commonly done using passive elements, but the large number of passives required to interface to a multi-standard single-chip radio increases the component count and size of the radio. Potential solutions to this problem are explored in this SET.

Time	Topic
8:00	**Multi-Mode Mobile Device Trends and Challenges** **Aarno Pärssinen,** *Nokia, Helsinki, Finland*
8:30	**Front-End Module and Filter Device Technology** **Rich Ruby,** *Avago Technologies, CA*
9:00	**CMOS PA Integration and Future RF Front-End Integration** **Donald McClymont,** *Axiom Microdevices, Irvine, CA*
9:30	**Integration of RF Front-End on SoC** **Hooman Darabi,** *Broadcom, Irvine, CA*

SE4: Unusual Data-Converter Techniques

Co-Organizer/Chair: **Venu Gopinathan**, *Bangalore, India*

Co-Organizer: **Boris Murmann**, *Stanford University, Stanford, CA*

Ever-increasing drive for higher speed, resolution, power in data converters, coupled with the need to coexist in ultra-short-channel technologies have spawned several fundamentally new techniques in the recent past. This evening session is aimed at addressing 4 such approaches. The first one tries to avoid explicit feedback for charge transfer, followed by the use of optics as a means for getting ultra-precise timing. Data conversion without aliasing (and hence smaller in-band quantization noise) is addressed by the third followed by time-to-digital conversion as a means to survive ultra-short-channel CMOS limitations. Experts in each of these areas will share their insights into the issues and discuss the various tradeoffs, advantages and disadvantages of these approaches.

Time	Topic
8:00	**Comparator and Zero-Crossing-Based ADCs: Challenges and Possible Solutions** **Hae-Seung Lee,** *MIT, Cambridge, MA*
8:30	**Optically Assisted Analog-to-Digital Conversion** **David Miller,** *Stanford University, Stanford, CA*
9:00	**Data Conversion and Digital Signal Processing without Sampling** **Yannis Tsividis,** *Columbia University, New York, NY*
9:30	**Time-to-Digital Converters: Opportunities in Nanometer CMOS** **Baher Haroun,** *Texas Instruments, Dallas, TX*

E1: Private Equity: Fight them or Invite them

Co-Organizer/ Moderator: **Sreedhar Natarajan,** *TSMC Design Technology, Kanata, Canada*
Co-Organizer: **Nicky Lu,** *Etron Technology, Hsinchu, Taiwan*

Lately, private equity firms have been purchasing companies for revenue generation. This panel will debate the role of private equity firms in the purchase and the survival of semiconductor companies. Typically, the private equity exit strategy is for short-term revenue generation through purchase and IPO. Will private equity continue to purchase companies and consolidate the industry?

The role of private equity has been likened to a double-edged sword. Many semiconductor companies thought being bought by a private equity firm was like being invaded; others have demonstrated the merits of being taken over. This panel will discuss the pros and cons of private equity firms and their role in creating mutually beneficial financial cooperation between the semiconductor industry and the financial community.

Panelists:

Tien Wu, Advanced Semiconductor Engineering (*ASE), Hsinchu, Tawain*
Paul Martin, *Former Prime Minister of Canada, Blackstone Group, New York, NY*
Jacques Benkoski, U.S. Venture Partners (*USVP), New York, NY*
Susumu Kohyama, *Toshiba Ceramics, Tokyo, Japan*
Ray Bingham, *General Atlantic, Palo Alto, CA*
Fu Chieh Hsu, *TSMC, Hsinchu, Tawain*

SE5: Trusting Our Lives to Sensors

Organizer: **Johannes Solhusvik,** *Micron, Oslo, Norway*

Chair: **Tim Denison,** *Medtronic Neurological, Columbia Heights, MN*

In this session we will highlight challenges associated with designing sensors used in life-critical applications. This is a hot topic since more and more applications rely on sensors, including automobiles, machines, aerospace, medicine, industry and robotics. No sensor is perfect, given signal-to-noise ratio and reliability limitations. So how do we ensure that a sensor is safe to use? We invite 4 renowned speakers to present their insight on this subject. Examples from automotive and medical sensing will be covered.

Time	Topic
8.00	**Crash Sensor Development Issues in Automotive Electronic Airbag Systems for Passenger Protection** **Young-Ho Cho,** *KAIST, Daejeon, Korea*
8.30	**Are Novel Sensor Technologies to be Trusted?** **Arndt Bußmann,** *Helion, Duisburg, Germany*
9.00	**Sensor and Control Algorithm Challenges for Building an Artificial Pancreas** **Bill Van Antwerp,** *Medtronic MiniMed, Northridge, CA*
9.30	**"BrainGate" Sensor for Interfacing Directly to the Brain – Lessons Learned with First Implants** **Arto Nurmikko,** *Brown University, Providence, RI*

MEDICAL & DISPLAYS

Chair: Reid Harrison, University of Utah, Salt Lake City, UT
Associate Chair: Oh-Kyong Kwon, Hanyang University, Seoul, Korea

8.1 An 8μW Heterodyning Chopper Amplifier for Direct Extraction of 2μV_{rms} Brain Biomarkers

8:30 AM

T. Denison[1], W. Santa[1], R. Jensen[1], D. Carlson[1], A-T. Avestruz[1,2], G. Molnar[1]
[1]Medtronic, Columbia Heights, MN
[2]MIT, Cambridge, MA

A chopper architecture using heterodyne frequency selection provides both amplification and flexible bandpower extraction of neural signals. The bandpass center frequency is tunable from DC to 500Hz and the filter BW is programmable from 5 to 25Hz using an on-chip 3rd-order LPF. The filter configuaration is stored in on-chip non-volatile memory. The 2μV_{rms} noise floor for a 10Hz band enables detection of key biomarkers. The "brain radio" including amplifiers, clocks and multipliers consumes 8μW from a 2V supply.

8.2 A 200μW Eight-Channel Acquisition ASIC for Ambulatory EEG Systems

9:00 AM

R. Yazicioglu[1,2], P. Merken[1], R. Puers[2], C. Van Hoof[1,2]
[1]IMEC, Leuven, Belgium
[2]K.U. Leuven, Leuven, Belgium

An ASIC for ambulatory EEG systems includes eight readout channels, an 11b ADC, a clock oscillator and a calibration signal generator, and has an electrode impedance measurement mode. The chopped instrumentation amplifier (IA) of the readout channel has 120dB CMRR, 1GΩ input impedance and 0.57μV_{rms} total noise in a 0.5 to 100Hz BW, while drawing 2.3μA from a 3V supply. The noise efficiency factor of the chopped IA is 4.1.

8.3 A Microsystem for Time-Resolved Fluorescence Analysis using CMOS Single-Photon Avalanche Diodes and Micro-LEDs

9:30 AM

B. Rae[1], C. Griffin[2], K. Muir[1], J. Girkin[2], E. Gu[2], D. Renshaw[1], E. Charbon[3], M. Dawson[2], R. Henderson[1]
[1]University of Edinburgh, Edinburgh, United Kingdom
[2]University of Strathclyde, Glasgow, United Kingdom
[3]Ecole Polytechnique Federale, Lausanne, Switzerland

A time-resolved fluorescence analysis system is designed in a 0.35μm high-voltage CMOS process. It incorporates a 100μm pitch 16×4 array of single-photon avalanche diodes with 9b in-pixel time-gated counters bump-bonded to an array of AlInGaN UV micro-LEDs. Synchronous time-gates and LED drive pulses are generated on chip with a 48ns range and resolution of 400ps. Accurate lifetime measurements of quantum dot samples have been achieved without dichroic filters.

Break **10:00 AM**

8.4 A CMOS Electro-Chemical DNA-Detection Array with On-Chip ADC

10:15 AM

F. Heer[1], M. Keller[1], G. Yu[2], J. Janata[2], M. Josowicz[2], A. Hierlemann[1]
[1]ETH Zurich, Zurich, Switzerland
[2]Georgia Institute of Technology, Atlanta, GA

A microsensor array with 576 electrodes and 24 channels is used for label-free detection of DNA hybridization. The chip is fabricated in a 0.6µm CMOS process with post processing. The readout channels use a 1st-order $\Delta\Sigma$ architecture, which uses the electrode-electrolyte capacitance as the integrator, resulting in a compact circuit. The measured linearity and SNR of the converter are both 11b. Experiments with short DNA samples and DNA extracted from human immunodeficiency virus (HIV) are presented.

8.5 A Fingerprint Sensor with Impedance Sensing for Fraud Detection

10:45 AM

T. Shimamura[1], H. Morimura[1], N. Shimoyama[1], T. Sakata[1], S. Shigematsu[1], K. Machida[2], M. Nakanishi[1]
[1]NTT, Atsugi, Japan, [2]NTT Advanced Technology, Atsugi, Japan

A capacitive large-scale fingerprint sensor IC integrates fingerprint sensing and an impedance sensing scheme to prevent spoofing with a fake finger. A test-chip is fabricated using a 0.5µm CMOS/sensor process. The difference between a living finger and a fake finger is detected by the test chip.

8.6 A 10b 75ns CMOS Scanning-Display-Driver System for QVGA LCDs

11:00 AM

I. Fujimori-Chen[1], R. Muller[2], W. Kan[1], M. Fazio[1], A. Farrell[1], D. Whitney[1]
[1]Analog Devices, Wilmington, MA
[2]University of California, Berkeley, CA

High-resolution displays require fast display drivers with low power and cost. We present a display driver in 0.35µm CMOS that operates on a single 3V battery for a 3.0-inch QVGA panel. The amplifier uses a slew current 100 times the quiescent current to settle a 300pF load in 75ns, while the DAC uses the common backplane voltage as a reference to achieve a DC accuracy less than 3mV. The video channel quiescent current draw is 850µA per channel and the area is 0.238mm^2.

8.7 A Direct-Type Fast Feedback Current Driver for Medium- to Large-Size AMOLED Displays

11:15 AM

J-Y. Jeon, Y-J. Jeon, Y-S. Son, K-C. Lee, H-M. Lee, S-C. Jung, K-H. Lee, G-H. Cho
KAIST, Daejeon, Korea

A direct-type fast feedback current driver with optimized frequency compensation and a pre-discharge function boosts the driving speed of medium- to large-size AMOLED displays. The driver is implemented in a 0.35µm CMOS technology and consumes 9.7µA of static current. The driving speed of 11µs is achieved for a full range of data transitions from 2.55µA to 10nA with data and feedback lines characterized by 1.5kΩ of series resistance and 100pF of shunt capacitance.

8.8 A Compact Low-Power CDAC Architecture for Mobile TFT-LCD Driver ICs

11:45 AM

Y-K. Choi, Z-Y. Wu, K. Kim, Y. Lee, M. Cho, H. Kim, D. Lee, W-G. Jung
Samsung Electronics, Yongin, Korea

A new capacitor-DAC architecture suitable for mobile TFT-LCD drivers uses less area than a resisitor-DAC (RDAC) and supports low power operation comparable to an RDAC. The architecture comprises three capacitors and one amplifier per channel. The amplifier draws less than 1µA of static current. The circuit is implemented for a 16M-color LCD driver IC with RGB-independent gamma control in a 0.13µm high-voltage CMOS process. The measured output deviation is 7mV and the measured DNL is 0.25LSB.

Conclusion **12:15 PM**

MM-WAVE & PHASED ARRAYS

Chair: Ali Hajimiri, California Institute of Technology, Pasadena, CA
Associate Chair: Kari Halonen, Technical University of Helsinki, Espoo, Finland

9.1 A 95GHz Receiver with Fundamental-Frequency VCO and Static Frequency Divider in 65nm Digital CMOS

8:30 AM

E. Laskin[1], M. Khanpour[1], R. Aroca[1], K. Tang[1], P. Garcia[2], S. Voinigescu[1]
[1]University of Toronto, Toronto, Canada
[2]STMicroelectronics, Crolles, France

A fully integrated receiver spanning the 76-to-95GHz band is designed in 65nm digital CMOS. The RX includes an LNA, a mixer, an IF amplifier, a fundamental-frequency VCO with buffers, and a divider with 50Ω driver, all consuming 206mW. Receiver operation up to 100°C is demonstrated with measured conversion gain of 12.5dB and NF of 7dB. The RX has an input P_{1dB} of -18dBm, and the VCO achieves a phase noise of -95dBc/Hz at 1MHz offset with total output power of +2dBm.

9.2 A Robust 24mW 60GHz Receiver in 90nm Standard CMOS

9:00 AM

B. Afshar, Y. Wang, A. Niknejad
University of California, Berkeley, CA

A highly integrated 60GHz front-end receiver is implemented in 90nm digital CMOS. The front-end receiver has a wide gain-tuning range of 60dB and an average NF of 6.2dB while consuming 24mW from a 1V supply. An RF-to-IF conversion gain of 18dB is achieved using an LO power of -2.5dBm. The design methodology is robust and stable against process variations and features excellent agreement between measured and simulated performance.

9.3 A 52GHz Phased-Array Receiver Front-End in 90nm Digital CMOS

9:30 AM

K. Scheir[1,2], S. Bronckers[1,2], J. Borremans[1,2], P. Wambacq[1,2], Y. Rolain[2]
[1]IMEC, Heverlee, Belgium
[2]Vrije Universiteit Brussel, Brussels, Belgium

A 52GHz phased-array homodyne receiver front-end with 2 antenna paths is implemented in 90nm digital CMOS. The QVCO and phase selectors provide control over the phase of the LO-signals, allowing beamforming and steering. The receiver achieves a conversion gain of 30dB/path and an NF of 7.1dB/path, yielding a system NF of 4.1dB. The chip consumes 65mW and occupies 0.1mm^2.

Break 10:00 AM

9.4 A Scalable 6-to-18GHz Concurrent Dual-Band Quad-Beam Phased-Array Receiver in CMOS

10:15 AM

S. Jeon, Y-J. Wang, H. Wang, F. Bohn, A. Natarajan, A. Babakhani, A. Hajimiri
California Institute of Technology, Pasadena, CA

A 6-to-18GHz integrated phased-array receiver is implemented in 0.13µm CMOS and is designed for scalability to very large arrays. It concurrently forms four beams at two different frequencies between 6 and 18GHz. Each receiver element achieves worst-case cross-polarization and cross-band rejections of 63.4dB and 48.8dB, respectively, over the entire band. A four-element phased array provides array patterns with peak-to-null ratio of 23dB and total array gain of 27.7dB at 18GHz.

9.5 A Near-Field Modulation Technique Using Antenna-Reflector Switching

10:45 AM

A. Babakhani, D. Rutledge, A. Hajimiri
California Institute of Technology, Pasadena, CA

Changing the antenna boundary condition using an array of reflectors and switches can efficiently generate independent signal constellations in different directions to create a secure communication link or send multiple data streams in various directions, as shown with a 60GHz proof of concept.

9.6 A 60GHz CMOS Receiver Using a 30GHz LO

11:15 AM

A. Parsa, B. Razavi
University of California, Los Angeles, CA

A double-conversion heterodyne receiver uses a polyphase filter in the RF path and two sets of downconversion mixers driven by a differential 30GHz LO. Fabricated in 90nm CMOS, the receiver achieves an NF of 5.7 to 8.8dB, a gain of 18.3 to 22dB, and I/Q mismatch of 1.1dB/2.1°. The circuit consumes 36mW from a 1.2V supply.

9.7 A 22.3dB-Voltage-Gain 6.1dB-NF 60GHz LNA in 65nm CMOS with Differential Output

11:45 AM

C. Weyers, P. Mayr, J. Kunze, U. Langmann
Ruhr-Universität Bochum, Bochum, Germany

A 60GHz 65nm CMOS LNA with a single-ended input and differential outputs achieves 22.3dB of voltage gain, a measured NF of 6.1dB and an S_{11}<-10dB over the 3dB bandwidth of 7.7GHz. The chip occupies 0.46×0.46mm^2 and interstage matching of two cascode amplifier stages and a buffer is realized by a balun and a transformer. The circuit consumes 35mW from a 1.2V supply.

9.8 A 2kV-ESD-Protected 18GHz LNA with 4dB NF in 0.13µm CMOS

12:00 PM

Y. Cao[1], V. Issakov[2], M. Tiebout[3]
[1]Infineon, Munich, Germany
[2]University of Paderborn, Paderborn, Germany
[3]Infineon, Villach, Austria

A differential 18GHz LNA is realized in 0.13µm CMOS and occupies 0.24mm^2. Measured performance of the mounted chip, including bond-wires, shows an NF of 4dB and a gain of 20dB at 18GHz. The 3dB bandwidth is 1.7GHz. IIP3 is -5dBm, all at a power consumption of 36mW from a single 1.5V supply.

9.9 A Broadband Distributed Amplifier with Internal Feedback Providing 660GHZ GBW in 90nm CMOS

12:15 PM

A. Arbabian, A. Niknejad
University of California, Berkeley, CA

A broadband distributed amplifier with an internal feedback is demonstrated in standard digital 90nm CMOS (f_t =100GHz) operating with a 1.2V supply. With the gain-boosting feedback in place, a passband average gain of 19dB with a 74GHz 3dB-cutoff is measured, providing 660GHz of GBW. The 0dB bandwidth of the amplifier is at 84GHz with the input and output matching better than 9dB up to 84GHz. The 1.19mm^2 chip consumes 84mW.

Conclusion **12:30 PM**

CELLULAR TRANSCEIVERS

Chair: Tony Montalvo, Analog Devices, Raleigh, NC
Associate Chair: Aarno Pärssinen, Nokia, Helsinki, Finland

10.1 A Fractional-Spur-Free ADPLL with Loop-Gain Calibration and Phase-Noise Cancellation for GSM/GPRS/EDGE

8:30 AM

H-H. Chang, P-Y. Wang, J-H. C. Zhan, B-Y. Hsieh
MediaTek, HsinChu, Taiwan

A 3.2-to-4GHz fractional-spur-free ADPLL is presented. Fractional spurs are first reduced by digital filtering with digital loop-gain calibration and then further suppressed by digital phase-noise cancellation. A cyclic time-to-digital converter enlarges the DR up to 31ns without significant area overhead. All fractional spurs are under the phase-noise level. The close-in reference spur is -84dBc and the phase noise at 400kHz offset is -117dBc/Hz, thus meeting GSM/GPRS/EDGE system requirements.

10.2 Single-Chip Tri-Band WCDMA/HSDPA Transceiver without External SAW Filters and with Integrated TX-Power Control

9:00 AM

B. Tenbroek[1], J. Strange[1], D. Nalbantis[1], C. Jones[1], P. Fowers[1], S. Brett[1], C. Beghein[1], F. Beffa[2]
[1]Analog Devices, West Malling, United Kingdom
[2]Federico Beffa Engineering, Agno, Switzerland

A fully integrated 0.18µm CMOS tri-band WCDMA/HSDPA TRX is presented. The RX front-end uses an RF notch filter and a passive mixer to achieve >+65dBm out-of-band IIP2, -2dBm out-of-band IIP3, and 2.8dB NF. The total RX current including the synthesizer is 35mA. The RX NF is 3.0dB with a -26dBm WCDMA TX blocker at its LNA input and desensitization due to an additional -45dBm CW out-of-band blocker at 0.5× or 2× the duplex offset frequency is around 2dB. The TRX uses an integrated TX power control with a true-rms-power detector, which achieves 30dB DR, ±0.3dB relative accuracy, ±1.5dB absolute accuracy, and a 15µs measurement time.

10.3 Equalization of IM3 Products in Wideband Direct-Conversion Receivers

9:30 AM

E. Keehr, A. Hajimiri
California Institute of Technology, Pasadena, CA

A SAW-less direct-conversion receiver system is presented, which uses a mixed-signal feedforward path to regenerate and equalize IM3 products. While the uncorrected system has an IIP3 of -8.6dBm, equalization yields 21.4dB of output IM3 reduction under worst-case UMTS blocker conditions.

Break **10:00 AM**

10.4 A Fully-Integrated Quad-Band GPRS/EDGE Radio in 0.13µm CMOS

10:15 AM

H. Darabi, A. Zolfaghari, H. Jensen, J. Leete, B. Mohammadi, J. Chiu, T. Li, Z. Zhou, P. Lettieri, Y. Chang, A. Hadji, P. Chang, M. Nariman, I. Bhatti, A. Medi, L. Serrano, J. Welz, K. Shoarinejad, S. Hasan, J. Castaneda, J. Kim, H. Tran, P. Kilcoyne, R. Chen, B. Lee, B. Zhao, B. Ibrahim, M. Rofougaran, A. Rofougaran
Broadcom, Irvine, CA

A fully integrated quad-band radio in 0.13µm CMOS, intended for GSM/GPRS/EDGE applications, consumes 140mW in the receive mode and 285mW in the transmit mode. The low-IF receiver achieves an NF of 2.5dB and an IIP3 of -11dBm. The polar transmitter achieves an 8PSK 400kHz mask of 60dBc, and the corresponding EVM is 3.2/2.2% for high/low bands. The GMSK mask is 65/69dBc with a phase error of 1.7/1.2°.

10.5 A 24mm² Quad-Band Single-Chip GSM Radio in 90nm Digital CMOS

10:30 AM

R. Staszewski, K. Muhammad, D. Leipold, O. Eliezer, M. Entezari, I. Bashir, C-M. Hung, J. Wallberg, R. Staszewski, P. Cruise, S. Rezeq, S. Vemulapalli, N. Barton, M-C. Lee, C. Fernando, K. Maggio, T. Jung, I. Elahi, S. Larson, T. Murphy, I. Deng, T. Mayhugh, Y-C. Ho, C. Lin, J. Jaehning
Texas Instruments, Dallas, TX

A 24mm² single-chip quad-band GSM radio in 90nm digital CMOS draws 56mA in receive mode and 47mA in transmit mode (with 7dBm output-power) from a 1.4V supply. It integrates the RF front-end with the digital baseband. The DSP/MPU clock coupling is reduced by running it on the RF oscillator clock. The PA and its driver are self calibrated by feeding their output back into the frequency reference and calculating statistics on the digital phase error signal.

10.6 Integration of a SiP for GSM/EDGE in CMOS Technology

10:45 AM

G. Li Puma[1], E. Kristan[1], P. De Nicola[2], C. Vannier[3], B. Greyling[4], S. Piccolella[5]
[1]Infineon Technologies, Duisburg, Germany, [2]Infineon Technologies, Sophia-Antipolis, France, [3]Infineon Technologies, Xi'an, China, [4]Infineon Technologies, Villach, Austria
[5]Infineon Technologies, Padova, Italy

A SiP for GSM/EDGE consists of two die, one includes the baseband and RF transceiver blocks and is fabricated in 0.13µm CMOS, and the other includes the power management unit and audio PA and is implemented in 0.25µm CMOS. Both die are flip-chipped into a 10×10mm² very thin PG-VF2BGA-293-1 package with a dual-layer substrate for routing. The integration of the power supply and battery management unit improves power efficiency and form factor.

10.7 A Low-Power WCDMA Transmitter with an Integrated Notch Filter

11:00 AM

A. Mirzaei, H. Darabi
Broadcom, Irvine, CA

A filtering technique to attenuate the receive-band noise enables a 65nm CMOS WCDMA transmitter to achieve an output noise level of -160dBc/Hz at 80MHz offset, while dissipating 65mW. Using a feedback filtering path, the circuit introduces a null with an arbitrary width at the receive frequency and eliminates the need for an external SAW filter.

10.8 A 1.2V 0.2-to-6.3GHz Transceiver with Less Than -29.5dB EVM@-3dBm and a Choke/Coil-Less Pre-Power Amplifier

11:15 AM

S. Kousai[1], D. Miyashita[1], J. Wadatsumi[1], A. Maki[2], T. Sekiguchi[1], R. Ito[1], M. Hamada[1]
[1]Toshiba, Kawasaki, Japan, [2]Toshiba, Yokohama, Japan

A 0.2-to-6.3GHz multi-mode radio transceiver is presented. Its choke/coil-less pre-PA achieves an EVM of less than -29.5dB for a 64QAM 54Mb/s OFDM signal at -3dBm over the entire frequency range of 0.2 to 7.2GHz. Input and output impedance matching of better than -9.2dB and -9.5dB are achieved without using external components.

10.9 A 24GHz Sub-Harmonic Receiver Front-End with Integrated Multi-Phase LO Generation in 65nm CMOS

11:45 AM

A. Mazzanti[1], M. Sosio[2], M. Repossi[3], F. Svelto[2]
[1]University of Modena and Reggio Emilia, Modena, Italy, [2]University of Pavia, Pavia, Italy
[3]STMicroelectronics, Pavia, Italy

A sub-harmonic architecture for wireless signal processing at Ka band is developed that results in power saving because the LO circuits operate at half the desired frequency and no IF stage is necessary. A 65nm CMOS prototype, including high-frequency front-end, baseband amplifier, multi-phase VCO, and dividers shows 31.5dB gain, 6.5dB NF, -17dBm IIP3, -90dBm LO re-irradiation at 24GHz while consuming 92mW.

Conclusion **12:15 PM**

OPTICAL COMMUNICATION

Chair: Larry DeVito, Analog Devices, Wilmington, MA
Associate Chair: Miki Moyal, Intel Israel, Haifa, Israel

11.1 A 2.7V 9.8Gb/s Burst-Mode TIA with Fast Automatic Gain Locking and Coarse Threshold Extraction

8:30 AM

T. De Ridder[1], P. Ossieur[2], B. Baekelandt[3], C. Mélange[3], J. Bauwelinck[1], C. Ford[4], X-Z. Qiu[1], J. Vandewege[1]
[1]Ghent University, Ghent, Belgium
[2]FWO Vlaanderen, Ghent, Belgium
[3]IWT Vlaanderen, Ghent, Belgium
[4]Centre for Integrated Photonics, Ipswich, United Kingdom

A 9.8Gb/s burst-mode TIA is implemented in a 0.25µm BiCMOS process. It uses a gain-locking mechanism that locks the gain to either 1800Ω or 600Ω within 4.5ns. At a BER of 10^{-10} and with 8B10B encoding, the receiver has a sensitivity of -14.0dBm and a DR of 12.2dB. The IC consumes 400mW from a 2.7V supply.

11.2 A 10Gb/s Laser-Diode Driver with Active Back-Termination in 0.18µm CMOS

9:00 AM

C-M. Tsai, M-C. Chiu
National Chiao Tung University, Hsinchu, Taiwan

A low-voltage circuit topology for active back-termination enables low-cost CMOS solutions. A diode-connected NMOS transistor with a feedback network provides back-termination capability. The chip has a modulation current range of 60mA. Measured rise/fall time and jitter are ~40ps and ~13ps_{pp}, respectively. The return loss for a 25Ω system is better than 8dB for a frequency range of DC to 8GHz. The IC consumes 240mW from a 1.8V supply.

11.3 A 20/10/5/2.5Gb/s Power-Scaling Burst-Mode CDR Using GVCO/Div2/DFF Tri-mode Cells

9:15 AM

C-F. Liang, S-I. Liu
National Taiwan University, Taipei, Taiwan

A 20/10/5/2.5Gb/s multi-band burst-mode CDR circuit is realized in 90nm CMOS technology. By using the GVCO/Div2/DFF tri-mode cells, the CDR can be configured by scaling power consumption for different input data rates. It occupies an active area of 0.2mm^2 and draws 90/60/43/27mW from a 1.2V supply.

11.4 A 10.3125Gb/s Burst-Mode CDR Using a ΔΣ DAC

9:30 AM

J. Terada[1], K. Nishimura[1], S. Kimura[2], H. Katsurai[1], N. Yoshimoto[2], Y. Ohtomo[1]
[1]NTT, Atsugi, Japan
[2]NTT, Chiba, Japan

A 10.3125Gb/s burst-mode CDR circuit is designed for 10G-EPON systems. A single gated VCO and ΔΣ modulator reduce frequency error to less than 2MHz and eliminate external devices. The CDR circuit achieves instantaneous locking in 1b, can tolerate a 160b sequence without transitions in the data, and has a jitter tolerance of over 0.27 UI_{pp}.

Break 10:00 AM

11.5 A 40Gb/s CDR Circuit with Adaptive Decision-Point Control Using Eye-Opening-Monitor Feedback

10:15 AM

H. Noguchi[1], N. Yoshida[1], H. Uchida[2], M. Ozaki[2], S. Kanemitsu[2], S. Wada[1]
[1]NEC, Kawasaki, Japan
[2]NEC Engineering, Kawasaki, Japan

A 0.18µm SiGe BiCMOS CDR circuit with an integrated eye-opening monitor enables adaptive control of a data decision point at over 40Gb/s. For a 30% duty-cycle-distorted signal of 53mV, the adaptive feedback acquired through 2D eye-monitoring improves the BER performance down to 10^{-12} compared with 2×10^{-7} with no adaptive control.

11.6 A 96Gb/s-Throughput Transceiver for Short-Distance Parallel Optical Links

10:45 AM

S. Goswami[1], T. Copani[1], B. Vermeire[1], H. Barnaby[1], G. Fetzer[2], R. Vercillo[2], S. Kiaei[1], A. Jain[1], H. Karaki[1]
[1]Arizona State University, Tempe, AZ
[2]Arete Associates, Tucson, AZ

A 96Gb/s optical transceiver for high-density processor-processor and processor-memory short-distance direct bus links is implemented in a 0.35µm SiGe BiCMOS process. The 64-channel transceiver has a 75µm inter-channel pitch and 21.3mW/Gb/s FOM. Electrical and substrate crosstalk are below -40dB across the BW.

11.7 A 90nm CMOS DSP MLSD Transceiver with Integrated AFE for Electronic Dispersion Compensation of Multi-mode Optical Fibers at 10Gb/s

11:15 AM

O. Agazzi[1,2], D. Crivelli[2], M. Hueda[2], H. Carrer[2], G. Luna[2], A. Nazemi[1], C. Grace[1], B. Kobeissy[1], C. Abidin[1], M. Kazemi[1], M. Kargar[1], C. Marquez[1], S. Ramprasad[1], F. Bollo[2], V. Posse[1], S. Wang[1], G. Asmanis[1], G. Eaton[1], N. Swenson[1], T. Lindsay[1], P. Voois[1]
[1]ClariPhy Communications, Irvine, CA
[2]ClariPhy Argentina, Cordoba, Argentina

A 32mm^2 90nm CMOS MLSD transceiver for electronic dispersion compensation of multi-mode optical fibers at 10Gb/s is presented. A 6b 10GS/s ADC feeds a parallel-processing DSP receiver. A sensitivity of -13.68dBm is demonstrated for the symmetric stressor of the IEEE 10GBASE-LRM standard in a line-card application with a 6-inch FR4 interconnect.

11.8 A 10Gb/s MLSE-based Electronic-Dispersion-Compensation IC with Fast-Power-Transient Management for WDM Add/Drop Networks

11:45 AM

H-M. Bae[1], J. Ashbrook[1], N. Shanbhag[2], A. Singer[2]
[1]Finisar, Champaign, IL
[2]University of Illinois at Urbana-Champaign, Urbana, IL

A 10Gb/s MLSE RX with fast power-transient management for optical add/drop multiplexer-based WDM networks is presented. The RX has a VGA with a fast AGC and a high-bandwidth offset-cancellation loop. Measured results indicate that the RX tolerates a 10dB/10µs optical-power transient with 72 consecutive identical digits with no BER impact, and offers a 100× improvement over a standard CDR in tracking an 8dB sinusoidal power transient at a BER of 10^{-4}.

Conclusion **12:15 PM**

HIGH-EFFICIENCY DATA CONVERTERS

Chair: Gabriele Manganaro, National Semiconductor, Salem, NH
Associate Chair: Tatsuji Matsuura, Renesas Technology, Gunma, Japan

12.1 An 820µW 9b 40MS/s Noise-Tolerant Dynamic-SAR ADC in 90nm Digital CMOS

8:30 AM

V. Giannini[1], P. Nuzzo[1], V. Chironi[2], A. Baschirotto[2], G. Van der Plas[1], J. Craninckx[1]
[1]IMEC, Leuven, Belgium
[2]University of Salento, Lecce, Italy

A 9b charge-sharing SAR ADC is presented that suppresses the comparator thermal noise through a redundant search algorithm and a noise-programmable comparator. A time-interleaved bootstrapped S/H enhances sampling speed and linearity guaranteeing 32MHz effective resolution bandwidth. The prototype in 90nm digital CMOS achieves 8.56 ENOB (53.3dB SNDR) at 40MS/s and consumes 820µW from a 1V supply, resulting in an FOM of 54fJ/conversion-step.

12.2 Highly-Interleaved 5b 250MS/s ADC with Redundant Channels in 65nm CMOS

9:00 AM

B. Ginsburg[1], A. Chandrakasan[2]
[1]Texas Instruments, Dallas, TX
[2]Massachusetts Institute of Technology, Cambridge, MA

A 36-channel interleaved 5b ADC demonstrates the use of parallelism in mixed-signal circuits to reduce the core supply voltage to 800mV and to improve energy efficiency. At 250MS/s, the total ADC power is 1.20mW, and the ENOB is 4.42 at the Nyquist rate. Six redundant channels counter yield loss from local variations in 65nm CMOS, and the yield of chips meeting the specification increases from 42% to 88%.

12.3 A 150MS/s 133µW 7b ADC in 90nm Digital CMOS Using a Comparator-Based Asynchronous Binary-Search Sub-ADC

9:30 AM

G. Van der Plas[1], B. Verbruggen[1,2]
[1]IMEC, Leuven, Belgium
[2]Vrije Universiteit Brussel, Brussels, Belgium

A fully dynamic 7b ADC uses a 2-step 1b-coarse and 6b-fine architecture. The 6b-fine converter is implemented using a comparator-based asynchronous binary-search architecture. The prototype implementation in 90nm digital CMOS with a 1V supply achieves 6.4 ENOB and 40dB SNDR (over the whole Nyquist band) at 150MS/s, yielding a 10fJ/conversion-step energy efficiency.

Break 10:00 AM

12.4 A 1.9µW 4.4fJ/conversion-step 10b 1MS/s Charge-Redistribution ADC

10:15 AM

M. van Elzakker[1,2], E. van Tuijl[1,2], P. Geraedts[1], D. Schinkel[1], E. Klumperink[1], B. Nauta[1]
[1]University of Twente, Enschede, Netherlands
[2]Philips Research, Eindhoven, Netherlands

A 10b SAR ADC uses a charge redistribution DAC, a two-stage comparator, and a delay-line-based controller. The ADC does not use any static bias current and power consumption is proportional to sample rate. At 1MS/s, the ADC uses 1.9µW. With 8.75 ENOB, the resulting FOM is 4.4fJ/conversion-step.

12.5 A 9.4-ENOB 1V 3.8µW 100kS/s SAR ADC with Time-Domain Comparator

10:45 AM

A. Agnes, E. Bonizzoni, P. Malcovati, F. Maloberti
University of Pavia, Pavia, Italy

A SAR ADC operating from 0.8V to 1.8V obtains a FOM of 56fJ/conversion-step with 1V supply. A time-domain comparator and two 6b capacitive split arrays with unity coupling capacitance are used. Second-harmonic distortion is -72dB and third-harmonic distortion is -78dB, with a single-ended architecture.

12.6 A 14b 100MS/s Pipelined ADC with a Merged Active S/H and First MDAC

11:15 AM

B. Lee[1], B. Min[2], G. Manganaro[2], J. W. Valvano[1]
[1]University of Texas, Austin, TX
[2]National Semiconductor, Salem, NH

A 14b 100MS/s pipelined ADC is implemented in a 0.18µm dual-gate-oxide CMOS technology. Low-power operation is achieved without sacrificing speed or accuracy by completely merging the active S/H into the first MDAC. The prototype ADC achieves 72.4dB SNR and 88.5dB SFDR at 100MS/s with a 46MHz input while consuming 230mW from a 3V supply.

12.7 A 1.2V 4.5mW 10b 100MS/s Pipelined ADC in 65nm CMOS

11:45 AM

M. Boulemnakher, E. Andre, J. Roux, F. Paillardet
STMicroelectronics, Crolles, France

A 10b pipelined ADC is implemented in a 65nm CMOS process. Using high-performance analog transistors, the circuit achieves 59dB SNDR and 74dB THD at 100MS/s. The 0.07mm^2 chip draws 3.7mA from a 1.2V supply.

12.8 A 2.2mW 5b 1.75GS/s Folding Flash ADC in 90nm Digital CMOS

12:00 PM

B. Verbruggen[1,2], J. Craninckx[1], M. Kuijk[2], P. Wambacq[1,2], G. Van der Plas[1]
[1]IMEC, Leuven, Belgium
[2]Vrije Universiteit Brussel, Brussels, Belgium

A 5b 1.75GS/s folding flash ADC in 90nm digital CMOS is presented. A dynamic folding technique is used to increase the resolution. The ENOB is 4.67 at low frequencies and >4.28 up to the Nyquist frequency with the ERBW extending up to 878MHz. The ADC draws 2.2mA from a 1.2V supply. The FOM is 50fJ/conversion-step.

Conclusion **12:15 PM**

MOBILE PROCESSING

Chair: Alice Wang, Texas Instruments, Dallas, TX
Associate Chair: Kazutami Arimoto, Renesas Technology, Hyogo, Japan

13.1 A Sub-1W to 2W Low-Power IA Processor for Mobile Internet Devices and Ultra-Mobile PCs in 45nm High-κ Metal-Gate CMOS

8:30 AM

G. Gerosa
Intel, Austin, TX

A 47M transistor, 25mm^2, sub-2W IA processor designed for mobile internet devices is presented. It features a 2-issue, in-order pipeline with 32KB iL1 and 24KB dL1 caches, integer and floating point execution units, x86 front end, a 512KB L2 cache and a 533MT/s front-side bus. The design is manufactured in 9M 45nm High-κ metal-gate CMOS and housed in a 441-ball µFCBGA package.

13.2 A 45nm 3.5G Baseband-and-Multimedia-Application Processor using Adaptive Body-Bias and Ultra-Low-Power Techniques

9:00 AM

G. Gammie, A. Wang, M. Chau, S. Gururajarao, R. Pitts, F. Jumel, S. Engel, P. Royannez, R. Lagerquist, H. Mair, J. Vaccani, G. Baldwin, K. Heragu, R. Mandal, M. Clinton, D. Arden, U. Ko
Texas Instruments, Dallas, TX

A 3.5G baseband (HSUPA/HSDPA, WCDMA, EDGE, GPRS, GSM) and multimedia applications processor uses a low-power digital and analog design platform and 45nm CMOS. The SoC contains an 840MHz ARM1176 and 480MHz TMS320C55x DSP, and uses power-management techniques including adaptive voltage scaling, adaptive body-bias, and a global/local blocking memory architecture. A unified methodology for simplifying power management integration is discussed.

13.3 A 65nm Single-Chip Application and Dual-Mode Baseband Processor with Partial Clock Activation and IP-MMU

9:30 AM

M. Naruse[1], T. Kamei[1], T. Hattori[1], T. Iriita[1], K. Nitta[1], T. Koike[1], S. Yoshioka[1], K. Ohno[1], M. Saigusa[2], M. Sakata[3], Y. Kodama[4], Y. Arai[5], T. Komura[6]
[1]Renesas Technology, Tokyo, Japan
[2]NTT DoCoMo, Tokyo, Japan
[3]Fujitsu Limited, Kanagawa, Japan
[4]Mitsubishi Electric, Hyogo, Japan
[5]Sharp, Hiroshima, Japan
[6]Sony Ericsson Mobile Communications, Tokyo, Japan

Supporting both WCDMA with HSDPA and GSM/GPRS/EDGE, the 9.3×9.3mm^2 IC, fabricated in triple-V_t 65nm CMOS, has 3 CPU cores and 21 separate power domains with partial clock activation that reduces power by 33.5%. An IP-MMU allows 17 media IPs to share the virtual memory space, reducing external memory by 20-80MB. 30fps-VGA video processing can be achieved under mixed virtual and physical address usage.

Break 10:00 AM

13.4 A 9.7mW AAC-Decoding, 620mW H.264 720p 60fps Decoding, 8-Core Media Processor with Embedded Forward-Body-Biasing and Power-Gating Circuit in 65nm CMOS Technology

10:15 AM

S. Nomura[1], F. Tachibana[1], T. Fujita[1], C. Kong Teh[1], H. Usui[1], F. Yamane[1], Y. Miyamoto[1], C. Kumtornkittikul[1], H. Hara[1], T. Yamashita[1], J. Tanabe[1], M. Uchiyama[1], Y. Tsuboi[1], T. Miyamori[1], T. Kitahara[1], H. Sato[1], Y. Homma[1], S. Matsumoto[2], K. Seki[2], Y. Watanabe[2], M. Hamada[1], M. Takahashi[1]

[1]Toshiba, Kawasaki, Japan

[2]Toshiba Microelectronics, Kawasaki, Japan

A power- and performance-scalable 8-core audio/visual processor is fabricated in 65nm CMOS consuming 620mW in H.264 720p 60fps decoding and 9.7mW in MPEG-4 AAC decoding. To reduce leakage currents during light workloads, three techniques are employed: an on-chip regulator that also works as a power-gating switch, an embedded forward body-biasing circuit reducing V_t variations, and a data-mapping FF. Symmetrical parallelization achieves binary compatible, 7.5× performance enhancement.

13.5 A 58mW 1.2mm² HSDPA Turbo-Decoder ASIC in 0.13µm CMOS

10:45 AM

C. Benkeser[1], A. Burg[1], T. Cupaiuolo[1], Q. Huang[1,2]

[1]ETH Zurich, Zurich, Switzerland

[2]Advanced Circuit Pursuit (ACP), Zollikon, Switzerland

A low-power 3GPP-HSDPA compliant turbo decoder is implemented in 0.13µm CMOS. The IC occupies 1.2mm² and dissipates 58mW from a 1V supply at a decoding rate of 10.8Mb/s, corresponding to an energy efficiency of 0.7nJ/b/iteration.

13.6 An 11mm² 70mW Fully-Programmable Baseband Processor for Mobile WiMAX and DVB-T/H in 0.12µm CMOS

11:15 AM

A. Nilsson, E. Tell, D. Liu

Linköping University, Linköping, Sweden

A fully programmable baseband processor for DVB-T/H and mobile WiMAX occupies 11mm² in 0.12µm CMOS, includes 1.5Mb of single port memory and 200kgates. A Single-Instruction stream Multiple Tasks (SIMT) architecture reduces control overhead and improves memory utilization. Measured power consumption for the highest data mode of 31.67Mb/s in DVB-T/H is 70mW at 70MHz surpassing both area and power figures of previous non-programmable DVB-T/H solutions.

Conclusion **11:45 AM**

EMBEDDED & GRAPHICS DRAM

Chair: Katsuyuki Sato, TSMC, Hsinchu, Taiwan
Associate Chair: Joo Sun Choi, Samsung Electronics, Gyeonggi-Do, Korea

14.1 A 500MHz Random-Access Embedded 1Mb DRAM Macro in Bulk CMOS

8:30 AM

S. Romanovsky[1], A. Katoch[1], A. Achyuthan[1], C. O'Connell[1], S. Natarajan[1], C. Huang[2], C-Y. Wu[2], M-J. Wang[2], C. Wang[2], P. Chen[2], R. Hsieh[2]
[1]TSMC Design Technology, Kanata, Canada
[2]TSMC, Hsinchu, Taiwan

A 1Mb embedded DRAM with V_{DD}-sensing and read-write synchronized with the sense amplifier turning on is described. Read and write operations for local sense amplifier are defined only by data from global bitlines. The reference generator for V_{DD} sensing uses charge sharing and does not require a DC source. The 1Mb macro with power supplies and ECC occupies 0.46mm^2 in 65nm CMOS and test-chip measurements confirm 500MHz operation.

14.2 A 170GB/s 16Mb Embedded DRAM with Data-Bus Charge-Recycling

9:00 AM

K. Hardee[1], M. Parris[1], F. Jones[1], D. Butler[1], G. Jones[1], M. Mound[1], T. Egging[1], T. Arakawa[2], K. Sasahara[2], K. Taniguchi[2], M. Miyabayashi[2]
[1]United Memories, Colorado Springs, CO
[2]Sony, Tokyo, Japan

A 1.0V 65nm 16Mb embedded DRAM test-chip demonstrates a total data rate of 170GB/s. Small-signal data busses with charge-recycling reduce power consumption by 57% to 680mW. Other features include hybrid early/late write, an output data FIFO and ECC with dynamic exclusive NOR gates.

14.3 A 2GHz 2Mb 2T Gain-Cell Memory Macro with 128GB/s Bandwidth in a 65nm Logic Process

9:30 AM

D. Somasekhar, Y. Ye, P. Aseron, S-L. Lu, M. Khellah, J. Howard, G. Ruhl, T. Karnik, S. Borkar, V. De, A. Keshavarzi
Intel, Hillsboro, OR

A 2Mb 2T PMOS gain-cell macro in a 65nm logic process has a bandwidth of 128GB/s with 2ns cycle time with 6-cycle latency at 2GHz. The macro features a full-rate pipelined architecture, ground precharge bitline, non-destructive read-out, partial write support and 128 row refresh to tolerate short refresh time. The cell is 2× denser than SRAM and is voltage compatible with logic.

Break 10:00 AM

14.4 An 833MHz Pseudo-Two-Port Embedded DRAM for Graphics Applications

10:15 AM

M. Kaku[1], H. Iwai[1], T. Nagai[1], M. Wada[1], A. Suzuki[1], T. Takai[1], N. Itoga[1], T. Miyazaki[1], T. Iwai[1], H. Takenaka[2], T. Hojo[1], S. Miyano[1], N. Ostuka[1]
[1]Toshiba, Kawasaki, Japan
[2]Toshiba Microelectronics, Kawasaki, Japan

We describe a pseudo-two-port embedded DRAM macro for graphics applications. It introduces read/write cross-point switch circuit and distributed steering redundancy switches for enabling concurrent read/write operation in two different banks. A 32Mb macro is characterized via a test-chip fabricated in 65nm embedded DRAM. A page-mode operating frequency of 833MHz at 1.2V is confirmed.

14.5 A 60nm 6Gb/s/pin GDDR5 Graphics DRAM with Multifaceted Clocking and ISI/SSN-Reduction Techniques

10:45 AM

S-J. Bae, Y-S. Sohn, K-I. Park, K-H. Kim, D-H. Chung, J-G. Kim, S-H. Kim, M-S. Park, J-H. Lee, S-Y. Bang, H-K. Lee, I-S. Park, J-S. Kim, D-H. Kim, H-R. Kim, Y-J. Shin, K-W. Yeom, J-Y. Lee, H-J. Yang, J. Choi, Y-H. Jun, K. Kim
Samsung Electronics, Hwasung, Korea

A 6Gb/s/pin 32b parallel 512Mb GDDR5 SDRAM is implemented using a 60nm DRAM process. To reduce ISI and SSN, an output data coding scheme, which includes data bus inversion, scrambling and a data preamble, is employed, increasing the eye width by 32ps at 6Gb/s. A fast-feedback DFE receiver with minimum overhead is also used. An adjustable clocking scheme with PLL on/off selection is implemented. The PLL has a programmable bandwidth, a replica delay and a locking cycle to minimize jitter.

14.6 Multi-Slew-Rate Output Driver and Optimized Impedance-Calibration Circuit for 66nm 3.0Gb/s/pin DRAM Interface

11:15 AM

D. Lee, S. Kang, N. Park, H. Lee, Y. Choi, J. Lee, S. Kwack, H. Lee, W. Yun, S. Shin, K. Kim, Y. Choi, Y. Yang
Hynix Semiconductor, Icheon, Korea

A multi-slew-rate output driver that covers supply voltage and C_{IO} variation improves data transfer speeds. An optimized impedance-calibration circuit is free from arbitrary impedance variation, and the code-shifter-based output driver configuration minimizes C_{IO} and layout area. A write-data-training method is also presented for accurate data receiving. The circuits and methods are implemented in 66nm 512Mb GDDR3(×32 I/O) SDRAM, and a data rate of 3.0Gb/s/pin is achieved.

14.7 A 0.1-to-1.5GHz 4.2mW All-Digital DLL with Dual Duty-Cycle-Correction Circuit and Update Gear Circuit for DRAM in 66nm CMOS

11:45 AM

W-J. Yun, H-W. Lee, D. Shin, S-D. Kang, J-Y. Yang, H-O. Lee, D-U. Lee, S. Shim, Y-J. Kim, W-J. Choi, K-S. Song, S-H. Shin, H-H. Choi, H-W. Moon, S-W. Kwack, J-W. Lee, Y-K. Choi, N-K. Park, K-W. Kim, Y-J. Choi, J-H. Ahn, Y-S. Yang
Hynix Semiconductor, Icheon, Korea

An all-digital DLL manufactured in 66nm CMOS has an update-gear circuit and a dual duty-cycle-correction circuit with clock receiver. This DLL corrects a duty-cycle error of 10% at t_{CK} of 3ns into 1% error with the combination of two DCCs and the clock receiver. With the help of the update gear circuit, the DLL operates at 1.5GHz with a 2.1V supply and consumes 4.2mW at 100MHz and 20mW at 1GHz with a 1.5V supply.

Conclusion **12:00 PM**

TD: TRENDS IN SIGNAL & POWER TRANSMISSION
Chair: William Bidermann, BK Associates, San Diego, CA
Associate Chair: Ken Shepard, Columbia University, New York, NY

15.1 A CMOS-SOI 2.45GHz Remote-Powered Sensor Tag

1:30 PM

S. Robinet, B. Gomez, N. Delorme
CEA-LETI/MINATEC, Grenoble, France

A 0.13µm CMOS-SOI remote-powered pressure sensor tag for ambient intelligence or healthcare applications integrates a 2.45GHz RFID front-end and a $\Delta\Sigma$ sensor readout interface for use with a capacitive pressure transducer. It exhibits a 12 ENOB resolution, a 100Hz measurement bandwidth, and a reading distance of 40cm.

15.2 A Triple-Band Passive RFID Tag

2:00 PM

A. Missoni[1], C. Klapf[1], W. Pribyl[1], H. Guenter[2], G. Holweg[2]
[1]Graz University of Technology, Graz, Austria, [2]Infineon, Graz, Austria

A CMOS rectifier switched to a charge pump with an efficiency of 69% at 550mV or a serial regulator generates a voltage of 0.7V to 1.6V in a frequency range from 1MHz to 2.5GHz. Dissipating 450nW the local oscillator frequency of typically 2.2MHz drifts in the voltage range of 0.55V to 1.8V by 5.4%. A boosting concept during HF TxD reduces the shunt transistor width by 2.5 and the chip input capacitance by 20%.

15.3 An Inductively Coupled 64b Organic RFID Tag operating at 13.56MHz with a Data Rate of 787b/s

2:30 PM

K. Myny[1], S. Van Winckel[1,2], S. Steudel[1], P. Vicca[1], S. De Jonge[1], M. Beenhakkers[3], C. Sele[3], N. van Aerle[3], G. Gelinck[4], J. Genoe[1], P. Heremans[1,2]
[1]IMEC, Leuven, Belgium, [2]K.U. Leuven, Leuven, Belgium, [3]Polymer Vision, Eindhoven, Netherlands, [4]TNO Science and Industry, Eindhoven, Netherlands

A 64b inductively coupled organic RFID tag on foil is demonstrated at 13.56MHz. The digital logic foil comprises 414 pentacene transistors and is powered by a pentacene double half-wave rectifier, connected to an inductive antenna. The data rate is 787b/s with load modulation behind the rectifier (DC). Also shown is a functional AC-modulated organic RFID tag.

Break 3:00 PM

15.4 A 107pJ/b 100kb/s 0.18µm Capacitive-Coupling Transceiver for Printable Communication Sheet

3:15 PM

L. Liu[1], M. Takamiya[1], T. Sekitani[1], Y. Noguchi[1], S. Nakano[1], K. Zaitsu[1], T. Kuroda[2], T. Someya[1], T. Sakurai[1]
[1]University of Tokyo, Tokyo, Japan, [2]Keio University, Yokohama, Japan

A 0.18µm CMOS transceiver for use with a printable 20×20cm^2 communication sheet enables capacitive coupling and point-to-point wired connections from TX to RX on the sheet. The transceiver, with data edge signaling and a DC-power-free pulse detector, achieves an energy efficiency of 107pJ/b at 100kb/s using wireless capacitive coupling communications with a wireline distance of 60cm.

15.5 A <5mW/Gb/s/link 16×10Gb/s Bi-Directional Single-Chip CMOS Optical Transceiver for Board-Level Optical Interconnects

3:45 PM

C. Schow[1], F. Doany[1], C. Chen[1,], A. Rylyakov[1], C. Baks[1], D. Kuchta[1], R. John[1], J. Kash[1]*
[1]IBM T.J. Watson, Yorktown Heights, NY
[*]Currently with the University of Illinois at Urbana-Champaign, Urbana, IL

A single-chip 0.13µm CMOS optical transceiver incorporates sixteen 10Gb/s transmitter and receiver channels for a 160Gb/s aggregate bit rate. The transceiver is designed to support chip-to-chip board-level optical data buses and consumes 4.65mW/Gb/s with an area efficiency of 9.4Gb/s/mm^2 per link.

15.6 Next-Generation Smart-Power Technologies — Challenges and Innovations Enabling Complex SoC Integration

4:15 PM

M. Tack[1], P. Moens[1], R. Gillon[1], J. Janssens[1], K. Geirnaert[1], J. Sevenhans[2]
[1]AMIS, Oudenaarde, Belgium, [2]AMIS, Vilvoorde, Belgium

Challenges and trends in high-voltage integrated circuits are described, with particular reference to the integration of power switches capable of handling up to 100V and 10A, electrical and thermal safe-operating areas, and proper thermal modeling of power drivers. The key benefits of next-generation technologies are illustrated for automotive and telecom applications.

15.7 An 11Gb/s Inductive-Coupling Link with Burst Transmission

4:45 PM

N. Miura[1], Y. Kohama[1], Y. Sugimori[1], H. Ishikuro[1], T. Sakurai[2], T. Kuroda[1]
[1]Keio University, Yokohama, Japan, [2]University of Tokyo, Tokyo, Japan

An 11Gb/s inductive-coupling link in 0.18µm CMOS demonstrates an energy efficiency of 1.4pJ/b and delivers a data rate 11× higher than previous inductive-coupling links. Communication distance is 5× longer than a capacitive-coupling link for the same data rate, layout area, and BER. Burst transmission at 6.4Gb/s reduces layout area by a factor of three.

15.8 A Capacitive Power-Management Circuit for Micropower Thermoelectric Generators with a 2.1µW Controller

5:00 PM

I. Doms[1,2], P. Merken[1,3], R. Mertens[1,2], C. Van Hoof[1,2]
[1]IMEC, Heverlee, Belgium, [2]K.U.Leuven, Heverlee, Belgium, [3]R.M.A., Brussels, Belgium

A compact power management circuit for thermoelectric generators as a power supply for on-the-body wireless sensor nodes is implemented in a 0.35µm CMOS process. The control circuit consumes 1.4µA to set the number of stages of a charge pump and to generate a 60kHz clock, leading to an overall efficiency of almost 60%.

15.9 A Full-Wave Rectifier for Interfacing with Multi-Phase Piezoelectric Energy Harvesters

5:15 PM

N. Guilar, R. Amirtharajah, P. Hurst
University of California, Davis, CA

A full-wave rectifier is fabricated in 0.35µm CMOS. Peak detection circuitry allows quadrature input phases from a multiple-electrode piezoelectric transducer to be rectified with reduced output ripple. The rectifier has a measured power efficiency of 98.3% while delivering 90µW and occupying 0.007mm^2.

Conclusion **5:30 PM**

LOW-POWER DIGITAL

Chair: Raj Amirtharajah, University of California, Davis, CA
Associate Chair: Holger Orup, Texas Instruments, Copenhagen, Denmark

16.1 iVisual: An Intelligent Visual Sensor SoC with 2790fps CMOS Image Sensor and 205GOPS/W Vision Processor

1:30 PM

C-C. Cheng[1], C-H. Lin[1], C-T. Li[1], S. Chang[1], C-J. Hsu[2], L-G. Chen[1]
[1]National Taiwan University, Taipei, Taiwan
[2]UMC, Hsinchu, Taiwan

iVisual, an intelligent visual sensor SoC integrating a 2790fps 128×128 CMOS image sensor and a 76.8GOPS, 374mW vision processor is implemented on a 7.5×9.4mm^2 die in a 0.18µm 2P4M CMOS image sensor process. An integrated feature processor increases average system throughput by 36%. The 205GOPS/W power efficiency is achieved by optimizing the PE cache and using resource clock gating.

16.2 A 125GOPS 583mW Network-on-Chip-Based Parallel Processor with Bio-inspired Visual-Attention Engine

2:00 PM

K. Kim, S. Lee, J-Y. Kim, M. Kim, D. Kim, J-H. Woo, H-J. Yoo
KAIST, Daejeon, Korea

A NoC-based parallel processor with a bio-inspired visual-attention engine (VAE) and 8 SIMD processing-element clusters achieves a peak performance of 125GOPS while dissipating 583mW from a 1.2V supply. The low-latency NoC employs dual-channel adaptive switching and packet-based clock gating, providing 76.8GB/s bandwidth. The cellular neural network with 2D shift-register array accelerates the VAE. The 36mm^2 chip contains 1.9M gates and 228KB SRAM in 0.13µm 8M CMOS.

16.3 A 360mW 105Mb/s DVB-S2-Compliant Codec based on 64800b LDPC and BCH Codes enabling Satellite-Transmission Portable Devices

2:30 PM

P. Urard[1], L. Paumier[2], V. Heinrich[1], N. Raina[3], N. Chawla[3]
[1]STMicroelectronics, Crolles, France
[2]STMicroelectronics, Grenoble, France
[3]STMicroelectronics, Noida, India

A 6.07mm^2 full DVB-S2 compliant (broadcast + interactive services) codec based on a 64,800b Low Density Parity Check (LDPC) and serially concatenated BCH code is presented. Error-free reception for HDTV is provided with a range of power dissipation from 100mW to 360mW at 135MHz (105Mb/s). The codec achieves up to 6.5× dynamic power reduction as compared to previous generations enabling satellite transmission for portable devices. This codec is realized in a 7M 65nm low-leakage CMOS technology.

Break 3:00 PM

16.4 A 512GOPS Fully-Programmable Digital Image Processor with full HD 1080p Processing Capabilities

3:15 PM

S. Arakawa[1], Y. Yamaguchi[2], S. Akui[1], Y. Fukuda[1], H. Sumi[1], H. Hayashi[1], M. Igarashi[1], K. Ito[2], H. Nagano[2], M. Imai[2], N. Asari[2]
[1]Sony, Atsugi, Japan
[2]Sony, Tokyo, Japan

FIESTA is a fully programmable processor capable of handling full HD 1080p digital images at 60fps. Fabricated in 65nm CMOS, the 12.8×11.94mm^2 die dissipates 784mW at 250MHz, which is equivalent to 115MOPS/mW, while the peak performance reaches 512 16b GOPS at 500MHz. The maximum power efficiency is 227MOPS/mW at 138GOPS. A 2MB multi-side transport (MST) memory is included along with power-gating and body-bias technologies.

16.5 A 242mW 10mm^2 1080p H.264/AVC High-Profile Encoder Chip

3:45 PM

Y-K. Lin, D-W. Li, C-C. Lin, T-Y. Kuo, S-J. Wu, W-C. Tai, W-C. Chang, T-S. Chang
National Chiao-Tung University, Hsinchu, Taiwan

A 1080p high profile H.264 encoder has a core area of 10mm^2 in 0.13µm CMOS and dissipates 242mW from 1.2V supply and 145MHz operating frequency. Compared to a state-of-the-art design targeted at 720p baseline, this design reduces power by 53.4% and area by 46.7% through parallelism-enhanced throughput and cross-stage-sharing pipeline.

16.6 A 320mV 56µW 411GOPS/Watt Ultra-Low-Voltage Motion-Estimation Accelerator in 65nm CMOS

4:15 PM

H. Kaul, M. Anders, S. Mathew, S. Hsu, A. Agarwal, R. Krishnamurthy, S. Borkar
Intel, Hillsboro, OR

A video motion-estimation engine for on-die acceleration of SAD computation in power-constrained mobile microprocessors is fabricated in 1.2V 65nm CMOS and occupies 0.089mm^2. Four-way speculation using dual 4:2 compressors and robust ultra-low-voltage circuits enable wide dynamic voltage range (1.4V to 230mV) with peak efficiency of 411GOPS/W measured at 320mV, deep subthreshold operation of 4.3MHz at 230mV consuming 14.4µW, and scalable performance up to 2.4GHz at 1.4V and 50°C.

16.7 A 65nm Sub-V_t Microcontroller with Integrated SRAM and Switched-Capacitor DC-DC Converter

4:45 PM

J. Kwong[1], Y. Ramadass[1], N. Verma[1], M. Koesler[2], K. Huber[2], H. Moormann[2], A. Chandrakasan[1]
[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Texas Instruments, Freising, Germany

A 65nm sub-V_t SoC integrates an on-chip, switched capacitor DC-DC converter with a 16b microcontroller and 128kb SRAM. The core logic is verified with a custom sub-V_t timing methodology. Functional down to 0.3V, the chip achieves 1µW standby power at minimum V_{dd}. The converter realizes above 75% efficiency at the minimum energy voltage of 0.5V.

Conclusion **5:15 PM**

WIDEBAND RECEIVERS

Chair: Jan Craninckx, IMEC, Leuven, Belgium
Associate Chair: David Ngo, RFMD

17.1 A Discrete-Time Mixing Receiver Architecture in 65nm CMOS with Wideband Harmonic Rejection

1:30 PM

Z. Ru, E. A. Klumperink, B. Nauta
University of Twente, Enschede, Netherlands

A discrete-time mixing architecture for software-defined radio receivers exploits 8× RF voltage oversampling followed by charge-domain weighting to achieve 40dB 3rd and 5th harmonic rejection without channel bandwidth limitations. Noise folding is also reduced by 3dB. A zero-IF downconverter chip in 65nm CMOS can receive RF signals from 200MHz to 900MHz, with NF_{min}=12dB, IIP3=11dBm at <20mW power consumption including multi-phase clock generation.

17.2 A Single-Inductor Dual-Band VCO in a 0.06mm^2 5.6GHz Multi-Band Front-End in 90nm Digital CMOS

2:00 PM

J. Borremans[1,2], S. Bronckers[1,2], P. Wambacq[1,2], M. Kuijk[2], J. Craninckx[1]
[1]IMEC, Leuven, Belgium
[2]Vrije Universiteit Brussel, Brussels, Belgium

A single-inductor 3.5-and-10GHz dual-band VCO achieves an FoM of 182dB, drawing between 1.8 and 8.3mA in all-digital 90nm CMOS. The VCO is embedded in a wideband front-end that achieves over 25dB gain up to 5.6GHz, a minimum NF of 4.5dB, draws less than 50mA from a 1.2V supply, and occupies 0.06mm^2.

17.3 A Wideband Balun LNA I/Q-Mixer Combination in 65nm CMOS

2:30 PM

S. Blaakmeer[1], E. Klumperink[1], D. Leenaerts[2], B. Nauta[1]
[1]University of Twente, Enschede, Netherlands
[2]NXP Semiconductors, Eindhoven, Netherlands

An inductor-less LNA-mixer topology merges an I/Q current-commutating mixer with a noise-canceling balun/LNA. The topology achieves >18dB conversion gain, a flat NF<5.5dB, IIP2=+20dBm and IIP3=-3dBm from 500MHz to 7GHz. The core circuit consumes 16mW and occupies less than 0.01mm^2 in 65nm CMOS.

Break 3:00 PM

TD: MOS MEDLEY

Chair: Glenn Gulak, University of Toronto, Toronto, Canada
Associate Chair: Werner Weber, Infineon Technologies, Munich, Germany

18.1 A 64/256-Element Thermopile Infrared-Sensor Chip with 4 Built-In Amplifiers for use in Atmospheric-Pressure Conditions

3:15 PM

H. Kawanishi[1], K. Hishinuma[2], M. Kimura[2], N. Motai[2], Y. Soutome[2], T. Tsukii[2], Y. Ishikawa[2], T. Katai[2], N. Hashiba[2]
[1]Seiko NPC, Tokyo, Japan, [2]Seiko NPC, Tochigi, Japan

64- and 256-element thermopile infrared focal-plane array chips with 4 built-in amplifiers are fabricated in a molybdenum-gate CMOS process with MEMS capabilities. The responsivity of a 64-element chip at 500K black-body temperature with no window is 146 to 195V/W. The 64-element chip is assembled in a compact TO-5 package with a Si-lens in air. It achieves 800μV/°C output with 200× amplification at 35°C black-body temperature, and a thermal time-constant of less than 2ms.

18.2 Measurement of Nano-Displacement Based on In-Plane Suspended-Gate MOSFET Detection Compatible with a Front-End CMOS Process

3:45 PM

E. Colinet[1], C. Durand[2,3], P. Audebert[1], P. Renaux[1], D. Mercier[1], L. Duraffourg[1], E. Ollier[1], F. Casset[1], P. Ancey[2], L. Bouchaillot[3], A. Ionescu[4]
[1]CEA-LETI, Grenoble, France, [2]STMicroelectronics, Crolles, France
[3]IEMN, Villeneuve d'Ascq, France, [4]EPFL, Lausanne, Switzerland

A 0.13μm CMOS chip with 250zF/√Hz equivalent capacitance noise is presented for measurement of NEMS displacement. Performance is increased by integrating on the same die the NEMS and its electronics. As an initial step toward full integration, an in-plane suspended gate MOSFET compatible with a front-end CMOS process is presented that shows 130zF/√Hz capacitance noise.

18.3 Ultra-Thin Chips on Foil for Flexible Electronics

4:15 PM

H. Rempp, J. Burghartz, C. Harendt, N. Pricopi, M. Pritschow, C. Reuter, H. Richter, I. Schindler, M. Zimmermann
Institute for Microelectronics, Stuttgart, Germany

Complex digital and mixed-signal circuits on 20μm-thin CMOS chips attached to foil and exposed to mechanical strain are demonstrated. The piezoelectric effect in the CMOS transistors will reduce the parametric yield in circuit designs based on tight process variations. Suppression of the effect is achieved by layout optimization, cancellation techniques or widening of the process corners.

18.4 A 0.18μm CMOS Integrated Sensor for the Rapid Identification of Bacteria

4:30 PM

N. Nikkhoo, C. Man, K. Maxwell, G. Gulak
University of Toronto, Toronto, Canada

A 1.03mm^2 integrated sensor fabricated in standard 0.18μm CMOS technology accurately identifies bacteria using the specificity of phages. The chip is capable of detecting a target bacterial strain in less than 10 minutes while consuming 122μW from a 3.3V supply. Integrated amplifiers having total input noise of 0.3pV^2/Hz at 1Hz amplify signals generated by on-chip top-layer metal electrodes that create nanowell trenches that collect intra-cellular ionic fluid.

Conclusion **4:45 PM**

PLLS & OSCILLATORS

Chair: Adrian Maxim, Silicon Laboratories, Austin, TX
Associate Chair: Changsik Yoo, Hanyang University, Seoul, Korea

19.1 A Low-Noise Wide-BW 3.6GHz Digital ΔΣ Fractional-*N* Frequency Synthesizer with a Noise-Shaping Time-to-Digital Converter and Quantization Noise Cancellation

1:30 PM

C-M. Hsu, M. Straayer, M. Perrott
Massachusetts Institute of Technology, Cambridge, MA

A 3.6GHz digital fractional-N synthesizer uses a gated-ring-oscillator time-to-digital converter and digital quantization-noise cancellation to achieve integrated phase noise less than 300fs (1kHz to 40MHz) with a BW of 500kHz. The synthesizer includes two 10b 50MHz passive DACs for digital control of the oscillator and an asynchronous frequency divider that avoids divide-value delay variation at its output.

19.2 Spurious-Tone Suppression Techniques Applied to a Wide-Bandwidth 2.4GHz Fractional-*N* PLL

2:00 PM

K. Wang[1], A. Swaminathan[2], I. Galton[1]
[1]University of California at San Diego, La Jolla, CA
[2]NextWave Wireless, San Diego, CA

Eliminating the ΔΣ modulator and adding a charge pump offset together suppress in-band fractional spurs in a 2.4GHz CMOS PLL by over 20dB to well below -60dBc. The PLL has a 975kHz bandwidth, a 12MHz reference, an on-chip sampled loop filter, a reference spur of -70dBc and worst-case phase noise of -121dBc/Hz at 3MHz offset.

19.3 A 3GHz Fractional-*N* All-Digital PLL with Precise Time-to-Digital Converter Calibration and Mismatch Correction

2:30 PM

C. Weltin-Wu[1], E. Temporiti[2], D. Baldi[2], F. Svelto[1]
[1]University of Pavia, Pavia, Italy
[2]STMicroelectronics, Pavia, Italy

A complete fractional all-digital PLL is implemented in standard 65nm CMOS, based on a time-to-digital converter with mismatch calibration and a frequency-doubled locking loop. The synthesizer features 95Hz frequency resolution and over a decade of bandwidth control, with an in-band plateau of -100dBc/Hz and worst case in-band spur of -45dBc, down from -36dBc when correction is active.

Break 3:00 PM

19.4 A 1GHz Fractional-*N* PLL Clock Generator with Low-OSR ΔΣ Modulation and FIR-Embedded Noise Filtering

3:15 PM

X. Yu, Y. Sun, L. Zhang, W. Rhee, Z. Wang
Tsinghua University, Beijing, China

A fractional-N PLL clock generator with less than 1ppm frequency resolution is implemented in 0.18μm CMOS. A hybrid FIR filtering technique enables low-OSR ΔΣ modulation by effectively suppressing the out-of-band quantization noise. The 1GHz PLL consumes 6.1mW and the active circuits occupy an area of 1mm^2.

19.5 A 90µW 12MHz Relaxation Oscillator with a -162dB FOM

3:45 PM

P. Geraedts, E. van Tuijl, E. Klumperink, G. Wienk, B. Nauta
University of Twente, Enschede, Netherlands

A relaxation oscillator exploits a noise filtering technique implemented with a switched-capacitor circuit to minimize phase noise. A 65nm CMOS design produces a sawtooth waveform, has a frequency tuning range of 1 to 12MHz and a constant frequency-tuning gain. By minimizing and balancing noise contributions from charge and discharge mechanisms, a FOM of -162dB is achieved, which is a 7dB improvement over state-of-the-art.

19.6 A 0.5-to-480MHz Self-Referenced CMOS Clock Generator with 90ppm Total Frequency Error and Spread-Spectrum Capability

4:15 PM

M. McCorquodale[1], S. Pernia[1], J. O'Day[1], G. Carichner[1], E. Marsman[1], N. Nguyen[2], S. Kubba[1], S. Nguyen[2], J. Kuhn[1], R. Brown[3]
[1]Mobius Microsystems, Detroit, MI
[2]Mobius Microsystems, Sunnyvale, CA
[3]University of Utah, Salt Lake City, UT

A self-referenced CMOS clock generator, configurable from 0.5 to 480MHz, is fabricated in a 0.25µm CMOS process and occupies 2.25mm^2. The clock generator is referenced to a compensated free-running 960MHz LC oscillator and achieves 90ppm total frequency error over process, voltage and temperature. At 24MHz it exhibits 6.5ps$_{rms}$ period jitter and consumes 49.5mW from a 3.3V supply.

19.7 A Temperature-Compensated Digitally-Controlled Crystal Pierce Oscillator for Wireless Applications

4:45 PM

S. Farahvash, C. Quek, M. Mak
Sirenza Microdevices, San Jose, CA

A temperature-compensated digitally controlled crystal oscillator (TC-DCXO) with frequency error less than 1ppm over the -30 to 80°C range is presented. The DCXO is based on a Pierce oscillator with two MIM capacitor arrays for tuning a 19.2MHz crystal with a resolution of 0.05ppm. The DCXO achieves such resolution by tuning the two switched-capacitor arrays in opposite directions with no $\Delta\Sigma$ modulation. The DCXO is implemented in 0.35µm SiGe BiCMOS and dissipates 6.5mW from a 2.7V supply.

Conclusion **5:15 PM**

WLAN/WPAN

Chair: Arya Behzad, Broadcom, San Diego, CA
Associate Chair: Tadashi Maeda, NEC, Kawasaki, Japan

20.1 A 1×2 MIMO Multi-Band CMOS Transceiver with an Integrated Front-End in 90nm CMOS for 802.11a/g/n WLAN Applications

1:30 PM

O. Degani, M. Ruberto, E. Cohen, Y. Eilat, F. Cossoy, N. Telzhensky, T. Maimon, G. Normatov, R. Banin, O. Ashckenazi, A. Ben-Bassat, S. Zaguri, G. Hara, M. Zajac, E. Shaviv, S. Wail, A. Fridman, S. Gross
Intel, Haifa, Israel

A 90nm CMOS RFIC for WLAN applications integrating LNAs, PAs, BB-filter and fractional-N synthesizer, both for 2.5GHz and 5GHz bands, is presented. A TX EVM of -28dB is achieved at output power (PA efficiency) of 15.5dBm (19%) and 14.5dBm (12%) for a 54Mb/s OFDM signal for low band and high band, respectively. An RX sensitivity of -74dBm is measured for 54Mb/s data rate.

20.2 A Dual-Band CMOS MIMO Radio SoC for 802.11n Wireless LAN

2:00 PM

L. Nathawad[1], M. Zargari[1], H. Samavati[2], S. Mehta[2], A. Kheirkhahi[1], P. Chen[1], K. Gong[1], B. Vakili-Amini[1], J. Hwang[2], M. Chen[2], M. Terrovitis[2], B. Kaczynski[2], S. Limotyrakis[2], M. Mack[2], H. Gan[2], M. Lee[2], S. Abdollahi-Alibeik[2], B. Baytekin[2], K. Onodera[2], S. Mendis[2], A. Chang[2], S. Jen[2], D. Su[2], B. Wooley[3]
[1]Atheros Communications, Irvine, CA, [2]Atheros Communications, Santa Clara, CA
[3]Stanford University, Stanford, CA

An 802.11n-draft-compliant 2×2 2-stream MIMO radio SoC incorporates two dual-band RF transceivers, analog baseband filters, data converters, digital PHY and MAC, and a PCI Express interface. Implemented in 0.13µm CMOS, it occupies 36mm^2. For 2.4GHz/5GHz, the receive chain NF is 4dB/6dB, and the transmit EVM is -34dBc/-30dBc at -5dBm output power.

20.3 A Fully-Digital 65nm CMOS Transmitter for the 2.4-to-2.7GHz WiFi/WiMAX Bands using 5.4GHz $\Delta\Sigma$ RF DACs

2:30 PM

A. Pozsgay[1], T. Zounes[2], R. Hossain[2], M. Boulemnakher[3], V. Knopik[3], S. Grange[4]
[1]STMicroelectronics, Plan-les-Ouates, Switzerland, [2]STMicroelectronics, La Jolla, CA
[3]STMicroelectronics, Crolles, France, [4]STMicroelectronics, Grenoble, France

A fully digital zero-IF 65nm CMOS transmitter is developed for connectivity applications in cellular handsets. It uses 3rd-order digital $\Delta\Sigma$ modulators and RF DACs, all clocked up to 5.4GHz. The circuit has 2.1% EVM at 2dBm rms output power with OFDM modulation, 64dB power control range, and a built-in signal generator, and occupies 0.4mm^2. A double-DAC structure is used for filtering the out-of-band noise, allowing coexistence with 2G/3G transceivers.

Break 3:00 PM

20.4 A Scalable 2.4-to-2.7GHz WiFi/WiMAX Discrete-Time Receiver in 65nm CMOS

3:15 PM

F. Montaudon[1], R. Mina[1], S. Le Tual[1], L. Joet[1], D. Saias[1], R. Hossain[2], F. Sibille[1], C. Corre[1], V. Carrat[3], E. Chataigner[1], J. Lajoinie[1], S. Dedieu[1], F. Paillardet[1], E. Perea[1]
[1]STMicroelectronics, Crolles, France, [2]STMicroelectronics, La Jolla, CA
[3]STMicroelectronics, Grenoble, France

A discrete-time WiFi/WiMAX RX includes I and Q ADCs. The RX complies to IEEE 802.16e and 802.11b/g/n, and achieves 4.8dB of NF and consumes 61mW in 65nm CMOS (77mW with PLL). The architecture uses one gain stage, a single 1st-order filter with built-in anti-alias capability and a parasitic correction loop. A SAR ADC shares the hardware of the filter, resulting in a merged SC structure from mixer to ADC.

20.5 A Single-Chip CMOS Radio SoC for v2.1 Bluetooth Applications

3:45 PM

D. Weber, W. Si, S. Abdollahi-Alibeik, M. Lee, R. Chang, H. Dogan, S. Luschas, P. Husted
Atheros Communications, Santa Clara, CA

A single-chip Bluetooth v2.1 SoC supporting EDR is implemented in standard 0.13µm CMOS. Area and power are reduced through the use of a polar transmitter with two-point modulation, a 500kHz low-IF receiver with 1st-order LPF, and a $\Delta\Sigma$ ADC with 74dB DR. Die area is 9.2mm^2, including 3.0mm^2 for analog and RF blocks. Continuous RX analog current draw is 29.7mA from a 1.2V supply.

20.6 A 0.6V 32.5mW Highly-Integrated Receiver for 2.4GHz ISM-Band Applications

4:15 PM

A. Balankutty, S-A. YU, Y. Feng, P. Kinget
Columbia University, New York, NY

A highly integrated ultra-low voltage 2.4-to-2.5GHz low-IF/zero-IF receiver consisting of an LNA, quadrature mixers, complex-band-pass/low-pass channel-select filters with gain control, a fractional-N LO synthesizer, and polyphase LO buffer has a maximum conversion gain of 67dB, an NF of 16dB, and an IIP3 of -10.5dBm. It consumes 32.5mW from a 0.6V supply and occupies 2.9mm^2 in 90nm CMOS.

20.7 A 5.4mW 0.07mm^2 2.4GHz Front-End Receiver in 90nm CMOS for IEEE 802.15.4 WPAN

4:45 PM

M. Camus[1,2], B. Butaye[1], L. Garcia[1], M. Sie[1], B. Pellat[1], T. Parra[2]
[1]STMicroelectronics, Crolles, France
[2]LAAS-CNRS, UPS Université de Paul-Sabatier, Toulouse, France

An 802.15.4-compliant 90nm CMOS 2.4GHz RX front-end includes all RF components, from the balun up to the first stage of the channel filter, and LO signal-conditioning blocks. It uses a 6MHz low-IF topology with an inductor-less LNA and an alternative clocking scheme for its passive mixer. It occupies 0.07mm^2 (0.23mm^2 including the input balun). The RX achieves 35dBv/dBm conversion gain, 7.5dB NF, -10dBm IIP3, and IR>32dB. It draws 4mA from a single 1.35V supply including the digital LO path.

20.8 A 2.4GHz 3.6mW 0.35mm^2 Quadrature Front-End RX for ZigBee and WPAN Applications

5:00 PM

A. Liscidini, M. Tedeschi, R. Castello
University of Pavia, Pavia, Italy

The front-end of a receiver compliant with the IEEE 802.15.4 (ZigBee) standard consumes 3.6mW from a 1.2V supply and has an active area of 0.35mm^2 in 90nm CMOS. Simultaneous power and area savings are achieved using only one integrated coil for the LNA, mixers, and VCO, and sharing the bias current among these blocks. The chip includes also a VGA and a complex filter/combiner with an image-rejection of 35dB.

20.9 A DDFS-Driven Mixing-DAC with Image and Harmonic Rejection Capabilities

5:15 PM

A. Maxim, R. Poorfard, M. Reid, J. Kao, C. Thompson, R. Johnson
Silicon Laboratories, Austin, TX

A 40-to-1000MHz mixing-DAC driven by a DDFS LO eliminates the need for off-chip LC tracking or SAW filters in wideband TV receivers front-end. It provides accurate quadrature LO phases, wide tuning range in small frequency steps, virtually instantaneous channel switching and negligible LO-to-RF leakage. Mixer specifications include IRR>65dB, HRR>73dB without using high selectivity filters, NF<16dB, IIP3>+20dBm, 0.15+0.2+0.1W mixers/DDFS/LO-path power dissipation and 1.2mm^2 die area.

Conclusion **5:30 PM**

SRAM

Chair: Hiroyuki Yamauchi, Fukuoka Institute of Technology, Fukuoka, Japan
Associate Chair: Peter Rickert, Texas Instruments, Dallas, TX

21.1 A 153Mb-SRAM Design with Dynamic Stability Enhancement and Leakage Reduction in 45nm High-κ Metal-Gate CMOS Technology

1:30 PM

F. Hamzaoglu[1], K. Zhang[1], Y. Wang[1], H. J. Ahn[1], U. Bhattacharya[1], Z. Chen[1], Y-G. Ng[1], A. Pavlov[1], K. Smits[2], M. Bohr[1]
[1]Intel, Hillsboro, OR
[2]Intel, Santa Clara, CA

A 153Mb SRAM that features a 0.346μm^2 cell is fabricated in 45nm high-κ metal-gate CMOS, achieving over 3.5GHz operation at 1.1V. The design uses integrated dynamic forward-body bias on the SRAM-cell PMOS to improve cell stability at low voltages. Dynamic sleep-transistor design is improved with active feedback control and on-die programmable voltage generator, reducing PVT variation. The subarray is also the building block of the 6MB L2 cache in next-generation Core™2 microprocessor.

21.2 A 450ps Access-Time SRAM Macro in 45nm SOI Featuring a Two-Stage Sensing-Scheme and Dynamic Power Management

2:00 PM

H. Pilo[1], V. Ramadurai[1], G. Braceras[1], J. Gabric[1], S. Lamphier[1], Y. Tan[2]
[1]IBM, Essex Junction, VT
[2]IBM, Hopewell Junction, NY

A 450ps access-time 512Kb SRAM macro is fabricated in 45nm SOI. Power improvements are achieved with little effect on performance and area. A two-stage, body-contacted sensing scheme along with other techniques achieve a 58% improvement in power consumption compared to the previous-generation macro. A single-device dynamic leakage-suppression scheme reduces leakage power by 37% with 1.8% area overhead and no wake-up cycle requirements.

21.3 A High-Density 45nm SRAM Using Small-Signal Non-Strobed Regenerative Sensing

2:30 PM

N. Verma, A. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

A high-density SRAM, composed of 0.25μm^2 cells in low-power 45nm CMOS, uses a non-strobed regenerative sense-amplifier that employs offset compensation and avoids strobe-timing uncertainty to increase read-access speed. Two 64kb arrays compare its performance to a conventional sense-amplifier, demonstrating a speed-up of up to 34%.

Break 3:00 PM

21.4 A Single-Power-Supply 0.7V 1GHz 45nm SRAM with a Asymmetrical Unit-β-Ratio Memory Cell

3:15 PM

A. Kawasumi[1], N. Otsuka[1], T. Yabe[1], Y. Takeyama[1], O. Hirabayashi[1], K. Kushida[1], A. Tohata[2], T. Sasaki[1], A. Katayama[1], G. Fukano[1], Y. Fujimura[1]
[1]Toshiba Semiconductor, Kawasaki, Japan
[2]Toshiba Microelectronics, Kawasaki, Japan

We present a bulk SRAM designed for GHz-class sub-1V operation, fabricated in 45nm bulk CMOS. Fine-grained bitline segmentation architecture and a unit β-ratio asymmetrical 6T memory cell are introduced to realize 1GHz operation at 0.7V. The asymmetrical cell saves 22% cell area compared with a conventional symmetrical cell.

21.5 A 65nm Low-Power High-Density SRAM Operable at 1.0V Under 3σ Systematic Variation Using Separate V_{th} Monitoring and Body Bias for NMOS and PMOS

3:45 PM

M. Yamaoka[1], N. Maeda[2], Y. Shimazaki[2], K. Osada[1]
[1]Hitachi, Tokyo, Japan
[2]Renesas Technology, Tokyo, Japan

A 1Mb SRAM is fabricated in 65nm low-power process with 0.51μm^2 cell. An NMOS and PMOS separately applied body-bias technique and NMOS and PMOS individual V_{th}-measurement method using leakage control are implemented in the prototype chip, which achieves 1.0V operation under 3σ systematic V_{th} variation.

21.6 A 100nm Double-Stacked 500MHz 72Mb Separate-I/O Synchronous SRAM with Automatic Cell-Bias Scheme and Adaptive Block Redundancy

4:15 PM

K. Sohn, Y-H. Suh, Y-J. Son, D-S. Yim, K-Y. Kim, D-G. Bae, T. Kang, H. Lim, S-M. Jung, H-G. Byun, Y-H. Jun, K. Kim
Samsung Electronics, Hwasung, Korea

A 500MHz 72Mb synchronous SRAM is implemented with 3 schemes to increase yield in a 100nm double-stacked SRAM cell technology. An automatic cell bias technique is used to control characteristics of cell transistors. Adaptive block redundancy efficiently deals with various types of defects. Wordline pulse-width regulation incorporated into the 2 schemes maximizes the SRAM operating frequency.

21.7 A 32kb 10T Subthreshold SRAM Array with Bit-Interleaving and Differential Read Scheme in 90nm CMOS

4:45 PM

I. Chang[1], J-J. Kim[2], S. Park[1], K. Roy[1]
[1]Purdue University, West Lafayette, IN
[2]IBM T.J. Watson, Yorktown Heights, NY

We demonstrate a 10T subthreshold SRAM with an efficient bit-interleaving structure for soft-error tolerance and a differential read scheme for improved stability. The 32kb (256×128) SRAM array is fabricated in 90nm CMOS and operates at 31.25kHz at 0.18V. With more aggressive wordline boosting, the V_{DD} can be reduced to 0.16V. At the minimum V_{DD} condition, the operating frequency is 500Hz and the power consumption is 0.123μW.

21.8 An Adaptively Dividable Dual-Port BiTCAM for Virus-Detection Processors in Mobile Devices

5:00 PM

C-C. Wang, C-J. Cheng, T-F. Chen, J-S. Wang
National Chung-Cheng University, Chia-Yi, Taiwan

We demonstrate an adaptively dividable dual-port BiTCAM in a virus-detection processor for mobile devices. The BiTCAM achieves a 48% power reduction and a 40% transistor reduction compared with conventional TCAMs. The 0.13μm processor with BiTCAM performs up to 3Gb/s virus detection at 0.44fJ/pattern-byte/scan.

Conclusion **5:15 PM**

TIMETABLE OF ISSCC 2008 SESSIONS

Sunday, February 3rd — ISSCC 2008 TUTORIALS

8 AM & 10 AM	**T1:** Class-D Audio Amplifiers **T2:** Pipeline ADCs **T3:** Temperature Sensors **T4:** SoC Power Reduction Techniques **T5:** Digital Phase-Locked Loops	12:30 PM & 2:30 PM	**T6:** Leakage Reduction Techniques **T7:** NAND Memories for SSD **T8:** Silicon mm-Wave Circuits **T9:** CMOS Biotechnology **T10:** High-Speed Chip-to-Chip Signaling

	MEMORY DESIGN FORUM	IMAGER DESIGN FORUM	GIRAFE DESIGN FORUM
8:00AM	**F1:** Embedded Memory Design for Nano-Scale VLSI Systems	**F2:** Wide-Dynamic Range Imaging	**F3:** Architectures & Circuit Techniques for Nanoscale RF CMOS

ISSCC 2008 EVENING SESSIONS

7:30PM	**SE1:** Green Electronics: Environmental Impacts, Power, E-waste		**SE2:** MEMS for Frequency Synthesis & Wireless RF Communications (Or Life without Quartz Crystal)

Monday, February 4th — ISSCC 2008 PAPER SESSIONS

8:15AM	**Session 1:** Plenary Session						
1:30PM	**Session 2:** Image Sensors & Technology	**Session 3:** Filters and Amplifiers	**Session 4:** Microprocessors	**Session 5:** High Speed Transceivers	**Session 6:** UWB Potpouri	**Session 7:** TD: Electronics for Life Sciences	
5:15PM	Social Hour: Poster Session - DAC and ASSC Student Design Contest Winners						

ISSCC 2008 EVENING SESSIONS

8:00PM	**SE3:** From Silicon to Aether and Back	**SE4:** Unusual Data Converter Techniques	**E1:** Private Equity: Fight Them or Invite Them	**SE5:** Trusting our Lives to Sensors

Tuesday, February 5th — ISSCC 2008 PAPER SESSIONS

8:30AM	**Session 8:** Medical & Displays	**Session 9:** mm-Wave & Phased Arrays	**Session 10:** Cellular Transceivers	**Session 11:** Optical Communication	**Session 12:** High-Efficiency Data Converters	**Session 13:** Mobile Processing	**Session 14:** Embedded & Graphics DRAM
1:30PM	**Session 15:** TD: Trends in Signal & Power Transmission	**Session 16:** Low-Power Digital	**Session: 17**: Wideband Receivers	**Session 18:** TD: MOS Medley	**Session 19:** PLLs & Oscillators	**Session 20:** WLAN/WPAN	**Session 21:** SRAM
5:15PM	Social Hour: Poster Session - DAC-ISSCC and ASSC Student Design Contest Winners						

ISSCC 2008 EVENING SESSIONS

8:00PM	**SE6:** Highlights of IEDM 2007	**SE7:** Trends & Challengers in Optical Communications Front-end	**E2:** Can Multicore Integration Justify the Increased Cost of Process Scaling?	

Wednesday, February 6th — ISSCC 2008 PAPER SESSIONS

8:30AM	**Session 22:** Variation Compensation & Measurement	**Session 23:** Non-Volatile Memory	**Session 24:** Analog Power Techniques	**Session 25:** Building Blocks for High-Speed Transceivers	**Session 26:** Wireless Frequency Generation	**Session 27:** ΔΣ Data Converters	
1:30PM	**Session 28:** Non-Volatile Memory & Digital Clocking	**Session 29:** TD: Trends in Communication Circuits & Systems	**Session 30:** Data Converter Techniques	**Session 31:** RF & mm-Wave Power Amplifiers	**Session 32:** MEMS & Sensors		

Thursday, February 7th — ISSCC 2008 SHORT COURSE

8:00AM	Embedded Power Management for IC Designers

	TD FORUM	ATAC DESIGN FORUM	MICROPROCESSOR FORUM	CIRCUIT DESIGN FORUM
8:00AM	**F4:** Power Systems from Gigawatts to Microwatts	**F5:** Future of High-Speed Transceivers	**F6:** Transistor Variability in Nanometer-Scale Technologies	**F7:** Digitally-Assisted Analog & RF Circuits

SE6: Highlights of IEDM 2007

Organizer: **Albert Theuwissen,** *Delft University of Technology, Delft, Netherlands/Harvest Imaging, Bree, Belgium*

Chairs: **Roland Thewes,** *Qimonda, Munich, Germany*
Ernesto Perea, *STMicroelectronics, Crolles, France*

Circuit-device interaction plays an increasingly important role in advanced CMOS technologies, so that for example, power and leakage aspects must be considered by circuit designers as well as in the technology development process. In this session, four papers presented at the International Electron Device Meeting (IEDM) in December 2007 are highlighted to the circuit-design community to discuss record performances, opportunities, and challenges that arise from advanced and extended CMOS processes.

Time **Topic**

8:00 **Localized SOI Technology : An Innovative Low Cost Self-Aligned Process for Ultra Thin Si-Film on Thin BOX Integration for Low Power Applications**

S. Monfray[1], M. Samson[1], D. Dutartre[1], T. Ernst[2], E. Rouchouze[1], D. Renaud[2], B. Guillaumot[1], D. Chanemougame[1], G. Rabille[1], S. Borel[2], J. Colonna[2], C. Arvet[1], N. Loubet[1], Y. Campidelli[1], J. Hartmann[2], L. Vandroux[2], D. Bensahel[1], A. Toffoli[2], F. Allain[2], A. Margin[1], L. Clement[3], A. Quiroga[1], S. Deleonibus[2], T. Skotnicki[1],
[1]STMicroelectronics, Crolles, France;
[2]CEA-LETI/MINATEC, Grenoble, France;
[3]NXP Semiconductor, Crolles, France

8:30 **A 32nm CMOS Low Power SoC Platform Technology for Foundry Applications with Functional High Density SRAM**

Shien-Yang Wu, J. J. Liaw, J. Y. Cheng, C. Y. Lin, M. C. Chiang, C. K. Yang, C. W. Chou, K. H. Pan, C. H. Yao, M. Y. Liu, L. C. Hu, C. H. Chang, S. Y. Chang, P. Y. Tong, Y. L. Hsieh, K. C. Ku, K. C. Lin, L. Y. Yeh, C. W. Chang, H. J. Lin, C. Chang, K. S. Chen, C. C. Chen, S. M. Cheng, S. H. Yang, Y. M. Sheu, M. T. Yang, H. C. Tseng, K. T. Huang, T. L. Lee, S. C. Chen, S. M. Jang, Y. C. See, M. S. Liang
TSMC, Hsinchu, Taiwan

9:00 **Record RF Performance of 45nm SOI CMOS Technology**

Sungjae Lee, Basanth Jagannathan, Shreesh Narasimha, Anthony Chou, Noah Zamdmer, Jim Johnson, Richard Williams, Lawrence Wagner, Jonghae Kim, Jean-Olivier Plouchart, John Pekarik, Scott Springer, Greg Freemanee
IBM, Essex Junction, VT

9:30 **A 45nm Logic Technology with High-k+ metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-Free Packaging**

K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Buechler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Pain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, B. McIntyre, P. Moon, J. Neirynck, C. Parker, D. Parsons, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Schifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, K. Zawadzki
Intel, Hillsboro, OR

SE 7: Trends and Challenges in Optical Communications Front-End

Co-Organizers: **Yuriy M. Greshishchev,** *Nortel, Ottawa, Canada*
Takuji Yamamoto, *Fujitsu Laboratories, Kawasaki, Japan*

Chair: **Naresh Shanbhag,** *University of Illinois, Urabana, IL*

Optical communications are undergoing revolutionary transformations with advances in electronic signal processing bringing improved system performance. Silicon technologies significantly extend the boundaries of digital signal processing versus analog and, what was impractical few years ago, is now close to production in optical systems. The areas where signal processing helps to improve optical systems are electronic dispersion compensation, advanced coding and detection techniques (for example, FEC and MLSE), and optical modems with coherent detection. A coherent optical system is no longer limited to the least spectral efficient OOK-modulation format, but is open to a wide variety of more efficient digital communications formats, such as QPSK, DQPSK, and QAM. What role will digital processing play at the existing and emerging data rates? What are the requirements for the components? Experts from industry and academia share their views on these topics

Time	Topic
8:00	**PON Propaedeutics** **David Bowler,** *Motorola, Lowell, MA*
8:20	**10Gb/s Optical Data Links With DSP-Based Dispersion Compensation** **Norman L. Swenson ,** *ClariPhy Communications, Irvine, CA*
8:40	**40Gb/s Optical Transport Milks DSP Technology** **John Sitch,** *Nortel, Ottawa, Canada*
9:00	**Signal Processing Challenges Towards 100G Optical Links** **Andrew Singer,** *University of Illinois, Urbana, IL*

E2: **Can Multicore Integration Justify the Increased Cost of Process Scaling?**

Organizer: **Thucydides Xanthopoulos**, *Cavium Networks, Marlboro, MA*

Co-Organizers: **Ana Sonia Leon**, *Sun Microsystems, Santa Clara, CA*
Samuel Naffziger, *AMD, Fort Collis, CO*
Vojin Oklobdzija, *University of Texas, Dallas TX*
Toru Shimizu, *Renesas Technology, Hyogo, Japan*

Moderator: **Don Draper**, *Rambus, Los Altos, CA*

In the last few years processors have hit the power wall and the GHz race is effectively over. Process scaling is yielding little more value than higher integration, providing more die space for extra components. At the same time, the design and manufacturing costs for more advanced processes have increased dramatically. The primary performance advantage of new process nodes has turned into integrating more and more CPU cores each generation. Yet integration issues, on-chip connectivity challenges, off-chip bandwidth demands, testing and software conspire to make this multi-core direction an expensive one in terms of design effort, time to market and platform challenges. How long will the benefits of core count expansion outweigh the costs?

Panelists:

Anant Agarwal, *MIT/ Tilera, Cambridge, MA*
Shekhar Borkar, *Intel, Hillsboro, OR*
Atsushi Hasegawa, *Renesas Technology, Tokyo, Japan*
Rick Hetherington, *Sun MIcrosystems, Sunnyvale, CA*
Brad McCredie, *IBM, Austin, TX*
Chuck Moore, *AMD,Sunnyvale, CA*

VARIATION COMPENSATION & MEASUREMENT

Chair: David Money Harris, Harvey Mudd College, Claremont, CA
Associate Chair: Hugh Mair, Texas Instruments, Dallas, TX

22.1 Razor II: In-Situ Error Detection and Correction for PVT and SER Tolerance

8:30 AM

D. Blaauw[1], S. Kalaiselvan[2], K. Lai[1], W-H. Ma[1], S. Pant[1], C. Tokunaga[1], S. Das[3], D. Bull[3]
[1]University of Michigan, Ann Arbor, MI, [2]AMD, Sunnyvale, CA
[3]ARM, Cambridge, United Kingdom

Traditional adaptive methods that compensate for PVT variations need safety margins and cannot respond to rapid environmental changes. We present a design (Razor II) that implements a latch with in-situ detection and architectural correction of variation-induced delay errors. Razor II also detects logic and register SER. A Razor II-enabled 64b processor implemented in 0.13µm CMOS has 33% lower power consumption than traditional DVS. SER tolerance is demonstrated with radiation experiments.

22.2 Energy-Efficient and Metastability-Immune Timing-Error Detection and Instruction-Replay-Based Recovery Circuits for Dynamic-Variation Tolerance

9:00 AM

K. Bowman[1], J. Tschanz[1], N. Kim[2], J. Lee[1], C. Wilkerson[1], S-L. Lu[1], T. Karnik[1], V. De[1]
[1]Intel, Hillsboro, OR, [2]Intel, Folsom, CA

A 65nm resilient-circuit test-chip implements energy-efficient and metastability-immune timing-error detection sequentials with an error-recovery design based on instruction replay to eliminate supply-voltage (V_{CC}) and temperature clock-frequency guardbands as well as to exploit path activation probability for maximizing throughput. Silicon measurements indicate that resilient circuits enable either 25 to 32% throughput gain at equal V_{CC} or 17% V_{CC} reduction at equal throughput.

22.3 A Process-Variation-Tolerant Floating-Point Unit with Voltage Interpolation and Variable Latency

9:30 AM

X. Liang, D. Brooks, G-Y. Wei
Harvard University, Cambridge, MA

We present two post-fabrication tuning techniques to reduce critical-path delay variations. Voltage interpolation can provide >30% delay tuning for a pipelined FPU fabricated in 0.13µm CMOS. Variable latency provides an additional 17% of tuning range. Measurements confirm that this interpolation scheme enables 15 chips with a 7% total frequency spread to operate at the median frequency.

22.4 A Commercial Field-Programmable Dense eFUSE-Array Memory with 99.999% Sense Yield for 45nm SOI CMOS

9:45 AM

G. Uhlmann[1], A. Aipperspach[1], T. Kirihata[2], C. Kothandaraman[2], Y. Li[2], C. Paone[1], B. Reed[1], N. Robson[2], J. Safran[2], D. Schmitt[1], S. Iyer[2]
[1]IBM, Rochester, MN, [2]IBM, Hopewell Junction, NY

A 99.999% sense-yield eFUSE supporting 0.6-to-1.2V read operation with in-hardware diagnostics for commercial VLSI design is implemented in a 64Kb one-time programmable-ROM test-chip. A 45nm SOI CMOS hardware reveals eFUSE programming ranges for V_{DD} of 1.0 to 1.6V and V_{PRG} of 1.2 to 1.8V with 99.999% yield.

Break **10:00 AM**

22.5 An All-Digital On-Chip Process-Control Monitor for Process-Variability Measurements

10:30 AM

F. Klass, A. Jain, G. Hess, B. Park
P.A. Semi, Santa Clara, CA

A 0.41mm^2 all-digital on-chip process-control monitor (PCM) for variability is implemented in 65nm dual-oxide triple-V_t CMOS. The PCM measurements translate directly into electrical design rules. The monitor consists of 4 modules: 1) an array racer measures timing races due to local mismatch, 2) a distributed jitter module measures supply-induced jitter, 3) a leaker module measures keeper ratios for dynamic circuits, and 4) a distributed ring oscillator measures across-the-die process variability.

22.6 Compact In-Situ Sensors for Monitoring Negative-Bias-Temperature-Instability Effect and Oxide Degradation

11:00 AM

E. Karl, P. Singh, D. Blaauw, D. Sylvester
University of Michigan, Ann Arbor, MI

Compact in-situ negative-bias temperature instability (NBTI) and oxide-degradation sensors with digital outputs are designed in 0.13µm CMOS. The 308µm^2 NBTI sensor and 150µm^2 oxide-degradation sensor provide convenient frequency outputs that can be used in standard-cell designs without additional analog references. The sensors allow large-scale monitoring of wear-out mechanisms to guide dynamic controls and warn of impending failure. The NBTI sensor provides V_t measurement with 3σ accuracy of 1.23mV across 40 to 110°C.

22.7 A Completely-Digital On-Chip Circuit for Local-Random-Variability Measurement

11:30 AM

R. Rao, K. Jenkins, J-J. Kim
IBM T.J. Watson, Yorktown Heights, NY

A 45nm SOI completely digital on-chip circuit to measure local random variation of FET currents is presented. The design uses an array of independently selectable upper devices arranged in a stacked configuration with a single bottom device. Using a voltage-to-frequency converter and an on-chip counter, the circuit eliminates analog current measurements and enables rapid, all-digital measurement of single FET variability.

22.8 1200µm^2 Physical Random-Number Generators Based on a SiN MOSFET for Secure Smart-Card Applications

12:00 PM

M. Matsumoto, S. Yasuda, R. Ohba, K. Ikegami, T. Tanamoto, S. Fujita
Toshiba, Kawasaki, Japan

A physical random number generator (RNG) based on a SiN MOSFET with a compact A/D converter is developed. Its circuit area is 1200µm^2 at 2Mb/s and 6000µm^2 at 10Mb/s. Furthermore, it generates high quality random numbers for the range of temperatures from -50 to 100°C.

22.9 A Charge-Injection-Based Active-Decoupling Technique for Inductive-Supply-Noise Suppression

12:15 PM

S. Pant, D. Blaauw
University of Michigan, Ann Arbor, MI

Increasing frequency and power/clock gating have worsened Ldi/dt drops while passive decap has become expensive due to leakage and area overhead. We demonstrate an all-digital under/overshoot detector combined with a switched-capacitor-based active circuit that uses nominal supply voltages to suppress Ldi/dt caused by rapid load transients, or during resonance. Measurements of a 0.13µm CMOS test-chip show 59% peak-noise reduction for ramp loads and 75% peak-noise reduction for resonance.

Conclusion 12:30 PM

NON-VOLATILE MEMORY

Chair: Giulio Casagrande, ST Microelectronics, Milano, Italy
Associate Chair: Shine Chung, TSMC, Hsinchu, Taiwan

23.1 A 34MB/s-Program-Throughput 16Gb MLC NAND with All-Bitline Architecture in 56nm

8:30 AM

R. Cernea[1], L. Pham[1], F. Moogat[1], J. Chan[1], B. Le[1], Y. Li[1], S. Tsao[1], T-Y. Tseng[1], K. Nguyen[1], J. Li[1], J. Hu[1], J. Park[1], C. Hsu[1], F. Zhang[1], T. Kamei[1], H. Nasu[1], P. Kliza[1], K. Htoo[1], J. Lutze[1], Y. Dong[1], M. Higashitani[1], J. Yang[1], H-S. Lin[1], V. Sakhamuri[1], A. Li[1], F. Pan[1], S. Yadala[1], S. Taigor[1], K. Pradhan[1], J. Lan[1], J. Chan[1], T. Abe[2], Y. Fukuda[2], H. Mukai[2], K. Kawakami[2], C. Liang[1], T. Ip[1], S-F. Chang[1], J. Lakshmipathi[1], S. Huynh[1], D. Pantelakis[1], M. Mofidi[1], K. Quader[1]
[1]Sandisk, Milpitas, CA
[2]Toshiba Semiconductor, Yokohama, Japan

A 16Gb MLC (4-state) NAND flash memory achieves a 34MB/s sustained program-throughput rate by using all memory cells available along a selected wordline and by using additional performance-enhancement techniques. The chip operating as an 8Gb binary device achieves a program throughput of over 60MB/s.

23.2 A 4b/Cell 8Gb NROM Data-Storage Memory with Enhanced Write Performance

9:00 AM

R. Sahar[1], A. Lavan[1], E. Geyari[1], A. Berman[1], I. Cohen[1], O. Tirosh[1], K. Danon[1], Y. Sofer[1], Y. Betser[1], A. Givant[1], A. Kushnarenko[1], Y. Horesh[1], R. Eliyahu[1], B. Eitan[1], W. P. Jen[2], Y. Feng[2], L.Yao[2], K. Jin[2], K. Woo[2], C. Jing[2], Y. Jing[2], K. Oh[2], Y. Jiun[2]
[1]Saifun Semiconductor, Netanya, Israel
[2]SMIC, Shanghai, China

A 155mm^2 8Gb data-storage memory based on a 4b/cell nitride ROM (NROM) in 90nm CMOS is introduced. The design features a programming method in which all levels are programmed in parallel and an approach for regulating erase current, resulting in a large improvement of write performance. A read scheme together with a data-scrambling method is implemented to allow better immunity to data-pattern-related array effects and to minimize the cumulative program-erase cycling effect.

23.3 A 45nm Self-Aligned-Contact-Process 1Gb NOR Flash with 5MB/s Program Speed

9:30 AM

J. Javanifard, T. Tanadi, H. Giduturi, K. Loe, R. Melcher, S. Khabiri, N. Hendrickson, A. Proescholdt
Intel, Folsom, CA

A 1Gb NOR flash implemented in a 45nm self-aligned-contact process is presented. While delivering 5MB/s programming performance, the chip achieves over 50% cost-per-bit reduction over the previous technology node. Design effort concentrates on the periphery circuitry and design rules to reduce die size.

Break 10:00 AM

23.4 A 50nm 8Gb NAND Flash Memory with 100MB/s Program Throughput and 200MB/s DDR Interface

10:15 AM

D. Nobunaga[1], E. Abedifard[1], F. Roohparvar[1], J. Lee[1], E. Yu[1], A. Vahidimowlavi[1], M. Abraham[1], S. Talreja[2], R. Sundaram[2], R. Rozman[2], L. Vu[1], C. Chen[1], V. Chandrasekhar[1], R. Bains[2], V. Viajedor[1], W. Mak[1], M. Choi[1], D. Udeshi[2], M. Luo[1], S. Qureshi[1], J. Tsai[1], F. Jaffin[1], Y. Liu[1]
[1]Micron, San Jose, CA
[2]Intel, Folsom, CA

A 3.3V 8Gb 50nm NAND flash memory with a synchronous DDR interface is presented with a sustained 200MB/s read data rate and a sustained 100MB/s write data rate. These speeds are achieved by a DDR interface, a quad-plane architecture and fast programming of 160µs. Two interfaces are supported: the standard asynchronous and the new synchronous DDR. A 64-cell NAND string offsets the area increase of the quad-plane architecture to achieve 65% array efficiency.

23.5 A Multi-Level-Cell Bipolar-Selected Phase-Change Memory

10:45 AM

F. Bedeschi[1], R. Fackenthal[2], C. Resta[3], E. Donze[1], M. Jagasivamani[2], E. Buda[1], F. Pellizzer[1], D. Chow[2], A. Fantini[3], A. Calibrini[3], G. Calvi[3], R. Faravelli[3], G. Torelli[3], D. Mills[2], R. Gastaldi[1], G. Casagrande[1]
[1]STMicroelectronics, Agrate Brianza, Italy
[2]Intel, Folsom, CA
[3]University of Pavia, Pavia, Italy

A 128Mb (256Mb MLC) 90nm phase-change memory is presented. A multi-level programming algorithm is developed and embedded into the chip, demonstrating 2b/cell feasibility. Experimental results are presented for time zero and after 48h, 125°C bake and 100k erase/write cycles.

23.6 A 120mm^2 16Gb 4-MLC NAND Flash Memory with 43nm CMOS Technology

11:15 AM

K. Kanda[1], M. Koyanagi[1], T. Yamamura[1], K. Hosono[1], M. Yoshihara[1], T. Miwa[2], Y. Kato[2], A. Mak[3], J. Chan[3], F. Tsai[3], A. Cernea[3], B. Le[3], E. Makino[1], T. Taira[1], H. Otake[1], N. Kajimura[1], S. Fujimura[1], Y. Takeuchi[1], M. Itoh[1], M. Shirakawa[1], D. Nakamura[1], Y. Suzuki[1], Y. Okukawa[1], M. Kojima[1], K. Yoneya[1], T. Arizono[1], T. Hisada[1], S. Miyamoto[1], M. Noguchi[1], T. Yaegashi[1], M. Higashitani[3], F. Ito[2], T. Kamei[2], G. Hemink[2], T. Maruyama[1], K. Ino[1], S. Ohshima[1]
[1]Toshiba Semiconductor, Yokohama, Japan
[2]Sandisk, Yokohama, Japan
[3]Sandisk, Milpitas, CA

A 120mm^2 16Gb MLC NAND flash memory is developed using 43nm CMOS. The area is reduced by more than 9% by applying a 66 NAND strings with a control-gate-driver circuit and power bus on memory cell array. Thus, a 16Gb chip capable of fitting into a microSD memory card.

Conclusion **11:45 AM**

ANALOG POWER TECHNIQUES

Chair: Doug Smith, SMSC, Austin, TX
Associate Chair: Francesco Rezzi, Marvell Semiconductor, Pavia, Italy

24.1 A 1.2mW 1.6V_{pp}-Swing Class-AB 16Ω Headphone Driver Capable of Handling Load Capacitance up to 22nF

8:30 AM

V. Dhanasekaran, J. Silva-Martinez, E. Sanchez-Sinencio
Texas A&M University, College Station, TX

A load-capacitance-aware compensation scheme for 3-stage amplifiers is presented. A class-AB 16Ω headphone driver designed using this scheme in 0.13µm technology can handle capacitive loads from 1pF to 22nF while consuming as little as 1.2mW of quiescent power. It can deliver a maximum RMS power of 20mW to the load with -84.8dB THD and 92dB peak SNR, and it occupies 0.1mm^2.

24.2 A High-Performance Digital-Input Class-D Amplifier with Direct Battery Connection in a 90nm Digital CMOS Process

9:00 AM

S. Ramaswamy, G. Burra, B. Forejt, M. Burns, J. Joy, J. Krishnan
Texas Instruments, Dallas, TX

A high-performance fully integrated digital-input "direct battery connect" stereo class-D audio amplifier with no additional masks, implemented in both 90nm and 0.13µm digital CMOS processes is presented. The SNR over the audio bandwidth is 93dB, the THD is 82dB with a 4.5V_{pp} output and the PSRR is 95dB at 217Hz. The area per channel is 0.5mm^2 (90nm) and the maximum output power is 350mW into a 16Ω load at a maximum battery voltage of 4.8V.

24.3 A 1V 16.9ppm/°C 250nA Switched-Capacitor CMOS Voltage Reference

9:30 AM

C-Y. Hsieh[1], H-W. Huang[2], K-H. Chen[1], S-Y. Kuo[2]
[1]National Chiao Tung University, Hsinchu, Taiwan
[2]National Taiwan University, Taipei, Taiwan

A precision voltage reference achieves a 16.9ppm/°C TC for V_{OUT} while drawing 250nA from a 1V supply. The reference uses a switched-capacitor technique and is fabricated in a 0.35µm CMOS process. The temperature dependences of carrier mobility and channel-length modulation are completely suppressed. The line sensitivity is 0.76%/V and the PSRRs at 100Hz and 10MHz are -41dB and -17dB, respectively. The die area is 0.049mm^2.

Break 10:00 AM

24.4 An Auto-Selectable-Frequency Pulse-Width Modulator for Buck Converters with Improved Light-Load Efficiency

10:15 AM

T. Man, P. Mok, M. Chan
Hong Kong University of Science and Technology, Kowloon, Hong Kong

This modulator improves buck converter light-load efficiency by changing the switching frequency among a set of pre-defined frequencies. The frequencies are chosen so that the output spectrum of the converter with this modulator is the same as it would be if pulse-width modulation were used. This design is fabricated in a 0.35µm CMOS process, uses 1.4mm^2 and provides 90% peak efficiency at 300mA and 70% efficiency at 10mA.

24.5 A 0.9V 0.35µm Adaptively-Biased CMOS LDO Regulator with Fast Transient Response

10:30 AM

Y-H. Lam, W-H. Ki
Hong Kong University of Science and Technology, Kowloon, Hong Kong

An adaptively biased LDO regulator with 0.9V output utilizes a transient-enhanced current mirror. It is stabilized with a 1µF output capacitor and occupies 0.053mm^2 in 0.35µm CMOS. It can operate down to V_{DD} = 1.05V when sourcing a load current of 50mA with 99.67% current efficiency while drawing 4.04µA at no load. The output voltage variation is 6.6mV_{pp} when the load is switched between 0 and 50mA with 10ns rise and fall times.

24.6 A 4-Output Single-Inductor DC-DC Buck Converter with Self-Boosted Switch Drivers and 1.2A Total Output Current

10:45 AM

M. Belloni[1], E. Bonizzoni[1], E. Kiseliovas[2], P. Malcovati[1], F. Maloberti[1], T. Peltola[2], T. Teppo[2]
[1]University of Pavia, Pavia, Italy
[2]National Semiconductor, Oulu, Finland

A single-inductor four-output DC-DC buck converter is presented. The 0.5µm CMOS circuit provides four output voltages, which can be independently regulated from 0 to V_{DD}-0.5V. The supply voltage range is 2.3 to 5V and the total minimum and maximum currents are 0.15 and 1.2A, respectively, with a peak efficiency of 82%.

24.7 Load-Independent Control of Switching DC-DC Converters with Freewheeling Current Feedback

11:15 AM

Y-J. Woo[1], H-P. Le[2], G-H. Cho[2], G-H. Cho[1], S-I. Kim[3]
[1]KAIST, Daejeon, Korea
[2]JDA Technology, Daejeon, Korea
[3]LG Electronics, Pyungtaek, Korea

A single-inductor dual-output boost DC-DC converter with freewheeling current feedback is presented. The converter loop is independent of the output load, resulting in a fast transient response. The fabricated chip occupies 3.2mm^2 in a 0.5µm BiCMOS process and an efficiency of 80% is achieved at a total output power of 220mW with a switching frequency of 1MHz.

24.8 A 10MHz-Bandwidth 2mV-Ripple PA-Supply Regulator for CDMA Transmitters

11:45 AM

B. Bakkaloglu , C. Chu, S. Kiaei
Arizona State University, Tempe, AZ

A switch-mode regulator and a class-AB buffer in parallel function as a PA supply modulator and achieve 10MHz bandwidth and 2mV ripple. The resulting modulator is suitable for CDMA applications. High-frequency switch-mode regulator ripple is cancelled by a rail-to-rail class-AB amplifier. The combined regulator tracks the input signal envelope with less than 0.2% error and achieves a maximum efficiency of 82% with a bandwidth of 10MHz.

Conclusion **12:15 PM**

BUILDING BLOCKS FOR HIGH-SPEED TRANSCEIVERS

Chair: Wolfgang Pribyl, Graz University of Technology, Graz, Austria
Associate Chair: Jerry Lin, MStar Semiconductor, Hsinchu, Taiwan

25.1 A 27Gb/s Forwarded-Clock I/O Receiver Using an Injection-Locked LC-DCO in 45nm CMOS

8:30 AM

F. O'Mahony[1], S. Shekhar[2], M. Mansuri[1], G. Balamurugan[1], J. Jaussi[1], J. Kennedy[1], B. Casper[1], D. Allstot[2], R. Mooney[1]
[1]Intel, Hillsboro, OR, [2]University of Washington, Seattle, WA

A 27Gb/s forwarded-clock data receiver using an injection-lock LC-DCO is realized in 45nm CMOS technology. The injection-locked DCO deskews the clock across 1UI, rejects high-frequency injected clock jitter, and has a supply noise sensitivity of 16ps/V. The DCO and sampler occupy 0.015mm^2 and dissipate 15mW and 28mW, respectively, resulting in an overall power efficiency of 1.6mW/Gb/s.

25.2 An 800MHz -122dBc/Hz-at-200kHz Clock Multiplier based on a Combination of PLL and Recirculating DLL

9:00 AM

S. Gierkink
Conexant Systems, Red Bank, NJ

A clock multiplier combines the low spur levels of a PLL with the low phase-noise of a recirculating DLL. It has two pulses running around a ring: one sets the delay by means of a PLL, and the other is periodically updated, as in a recirculating DLL. The 0.048mm^2 90nm-CMOS circuit has -122dBc/Hz phase noise at 200kHz offset of an 800MHz carrier, -48dBc reference spur, and consumes 15mW from a 1V supply.

25.3 A 1ps-Resolution 2ns-Span 10Gb/s Data-Timing Generator with Spectrum Conversion

9:30 AM

T. Kawamura[1], Y. Ohtomo[1], K. Nishimura[1], N. Ishihara[2]
[1]NTT, Atsugi, Japan, [2]Gunma University, Kiryu, Japan

A data-timing generator (DTG) provides a delay of >2ns for DC-to-11Gb/s input data. By using a spectrum-conversion technique that suppresses the effect of the group-delay deviation, the output jitter is reduced to one-third that of a conventional DTG. The total jitter of 2ns-delayed 10Gb/s output data is 12ps$_{pp}$ including 7ps$_{pp}$ of input-data jitter. The DTG is fabricated using a 0.25µm SiGe BiCMOS process and consumes 2.5W from a 3.3V supply.

25.4 A 2.6mW 370MHz-to-2.5GHz Open-Loop Quadrature Clock Generator

9:45 AM

K-H. Kim[1], P. Coteus[1], D. Dreps[2], S. Kim[1], S. Rylov[1], D. Friedman[1]
[1]IBM T.J. Watson, Yorktown Heights, NY, [2]IBM, Austin, TX

An open-loop multi-octave quadrature clock generator that consists of cascaded quadrature correction stages is reported. It uses CMOS inverters. Fabricated in a 65nm CMOS process, the chip achieves frequency ranges of 1.2 octaves and 2.7 octaves for phase accuracies of ±2° and ±5°, respectively, and consumes 2.6mW from a 1V supply at 2.5GHz.

Break 10:00 AM

25.5 A 94GHz Locking-Hysteresis-Assisted and Tunable CML Static Divider in 65nm SOI CMOS

10:15 AM

D. Kim, J. Kim, C. Cho
IBM, Hopewell Junction, NY

A CML static divider operating up to 94.4GHz in 65nm SOI CMOS is presented. The operation range of the divider is extended by input-locking hysteresis and bias tuning. The locking hysteresis and sensitivity curve are analyzed, simulated, and measured. A 0.74dB hysteresis gain is observed. The divider consumes 15.8mW per flip-flop at 82.4GHz and the power-delay product per gate is 24fJ.

25.6 A 1.8W 115Gb/s Serial Link for Fully Buffered DIMM with 2.1ns Pass-Through Latency in 90nm CMOS

10:45 AM

D. Pfaff, S. Kanesapillai, V. Yavorskyy, C. Carvalho, R. Yousefi, M. Khan, T. Monson, M. Ayoub, C. Reitlingshoefer
Diablo Technologies, Gatineau, Canada

A low-latency 115Gb/s serial link for data communication between DIMMs is presented. With 24 unidirectional FBDIMM-standard-compliant 4.8Gb/s transceivers consuming 15mW/Gb/s, low-power advanced memory buffers are enabled. The serial link incorporates a 2ps-jitter CMU, $50mV_{pp\text{-}diff}$-sensitivity receivers, and single-tap transmit equalizers as well as a 200kHz-BW CDR accepting low transition density data patterns.

25.7 A 90nm CMOS Dual-Channel Powerline Communication AFE for Home-Plug AV with a Gb extension

11:15 AM

K. Findlater[1], T. Bailey[1], A. Bofill[2], N. Calder[1], S. Danesh[1,3], R. Henderson[3], W. Holland[1], J. Hurwitz[1], S. Maughan[3], A. Sutherland[1], E. Watt[1]
[1]Gigle Semiconductor, Edinburgh, United Kingdom, [2]Gigle Semiconductor, Barcelona, Spain, [3]University of Edinburgh, Edinburgh, United Kingdom

An integrated 90nm powerline communications AFE is presented. The AFE comprises a 2-to-28MHz 200Mb/s channel and also a wider band Gb-capable channel, which can operate simultaneously. Measurement results show that the AFE achieves sufficient linearity and noise performance when integrated as part of an SoC to achieve the required data rates.

25.8 A 3.5mW W-band Frequency Divider with Wide Locking Range in 90nm CMOS

11:45 AM

K-H. Tsai, L-C. Cho, J-H. Wu, S-I. Liu
National Taiwan University, Taipei, Taiwan

Two low-power wide-range injection-locked frequency dividers (ILFDs) are fabricated in 90nm CMOS technology. Two ILFDs have the locking range of 85.1 to 96.3GHz and 98.9 to 105.2GHz, respectively. The first and the second ILFDs consume 3.5mW and 3.3mW, respectively, from a 1.2V supply without buffers and bias circuits. Each ILFD has an area of $0.66\times0.51mm^2$ with pads.

25.9 An 8×3.2Gb/s Parallel Receiver with Collaborative Timing Recovery

12:00 PM

A. Agrawal[1], P. Hanumolu[2], G-Y. Wei[1]
[1]Harvard University, Cambridge, MA, [2]Oregon State University, Corvallis, OR

An 8×3.2Gb/s parallel receiver with collaborative timing recovery is realized in a 0.13µm 1P8M CMOS logic process. A global timing-recovery block that combines timing-error information from several parallel data channels more than doubles the jitter tolerance bandwidth while consuming <6.4mW/Gb/s from a 1.1V supply.

Conclusion **12:15 PM**

WIRELESS FREQUENCY GENERATION

Chair: Nikolaus Klemmer, Ericsson Mobile Platforms, Research Triangle Park, NC
Associate Chair: Chris Rudell, Intel, Santa Clara, CA

26.1 A 410GHz CMOS Push-Push Oscillator with an On-Chip Patch Antenna

8:30 AM

E. Seok, K. O
University of Florida, Gainesville, FL

A 410GHz push–push oscillator with an on-chip patch antenna is fabricated using low-leakage transistors of a 6M 45nm CMOS process. The chip area including buffers is 350×840μm^2 and excluding buffers is 390×640μm^2.

26.2 A 1.4mW 4.90-to-5.65GHz Class-C CMOS VCO with an Average FoM of 194.5dBc/Hz

9:00 AM

A. Mazzanti[1], P. Andreani[2]
[1]University of Modena and Reggio Emilia, Modena, Italy
[2]Lund University, Lund, Sweden

A class-C CMOS harmonic VCO maximizes the oscillation amplitude by operating the active devices operating in class C, while the bias-current noise is naturally rejected by the topology. Drawing 1.4mA from a 1V supply, the 0.13μm CMOS prototype exhibits an average phase noise of -130dBc/Hz at 3MHz offset over the 4.90-to-5.65GHz tuning range, for an FoM of 194.5dBc/Hz.

26.3 A 324GHz CMOS Frequency Generator Using a Linear-Superposition Technique

9:30 AM

D. Huang[1], T. LaRocca[1], L. Samoska[2], A. Fong[2], F. Chang[1]
[1]University of California, Los Angeles, CA
[2]Jet Propulsion Laboratory, Pasadena, CA

A 324GHz frequency generator is realized in 90nm CMOS based on linear superposition of phase-shifted fundamental signals at 81GHz. The technique minimizes the fundamental, 2nd and 3rd harmonics and results in a high fundamental-to-4th-harmonic signal-conversion efficiency of 17% (or -15.4dB). The prototype produces a calibrated output of -46dBm when biased at 1V using 12mA current.

26.4 A 1V 220MHz-Tuning-Range 2.2GHz VCO Using a BAW Resonator

9:45 AM

P. Vincent, J. David, I. Burciu, J. Prouvee, C. Billard, C. Fuchs, G. Parat, E. De Foucauld, A. Reinhardt
CEA-LETI-Minatec, Grenoble, France

A 1V broadband BAW-tuned VCO designed in 0.13μm CMOS is presented. The BAW VCO operates at 2.2GHz and achieves a frequency tuning range (FTR) of 10% with a phase noise of -135.7dBc/Hz at 1MHz offset. A tuning concept based on a fixed negative active capacitor and MOS varactors is described.

Break 10:00 AM

26.5 A 56-to-65GHz Injection-Locked Frequency Tripler with Quadrature Outputs in 90nm CMOS

10:15 AM

W. Chan[1], J. Long[1], J. Pekarik[2]
[1]Delft University of Technology, Delft, Netherlands
[2]IBM Microelectronics, Burlington, VT

A sub-harmonic injection-locked I/Q tripler is implemented in 90nm CMOS. The tripler test-chip consists of a negative-resistance gain cell and a hard limiter, and an optimized 50Ω output buffer. With a free-running frequency at 60.6GHz, the tripler can be locked from 56.5 to 64.5GHz with 0dBm RF input power. The measured phase-noise degradation compared to the input source is 9.2±1dB. The 0.3×0.3mm^2 tripler core (with passives) consumes 9.6mW (14.2mW in the output buffers) from a 1V supply.

26.6 A 28GHz Low-Phase-Noise CMOS VCO Using an Amplitude-Redistribution Technique

10:45 AM

Y. Wachi, T. Nagasaku, H. Kondoh
Hitachi, Tokyo, Japan

An amplitude-redistribution technique improves phase-noise performance of mm-wave cross-coupled VCOs by controlling a distribution of voltage swings on the oscillator nodes with a unique resonator configuration. A 28GHz VCO, implemented in 0.13µm CMOS, has a phase-noise performance of -112.9dBc/Hz at 1MHz offset and an FoM of -187.4dBc/Hz.

26.7 A 39.1-to-41.6GHz ΔΣ Fractional-N Frequency Synthesizer in 90nm CMOS

11:00 AM

S. Pellerano[1], R. Mukhopadhyay[2], A. Ravi[1], J. Laskar[3], Y. Palaskas[1]
[1]Intel, Hillsboro, OR
[2]Texas Instruments, Dallas, TX
[3]Georgia Institute of Technology, Atlanta, GA

A 39.1-to-41.6GHz 1.2V 64mW ΔΣ fractional-N frequency synthesizer is designed in 90nm CMOS. The 40GHz division is performed by a self-calibrated injection-locking divide-by-4 with less than 10mW. The synthesizer achieves 3kHz resolution with a 50MHz reference frequency. Measured phase noise at 1MHz offset is -90dBc/Hz.

Conclusion **11:15 AM**

ΔΣ DATA CONVERTERS

Chair: Zhongyuan Chang, IDT Technology, Shanghai, China
Associate Chair: Yiannos Manoli, University of Freiburg, Freiburg, Germany

27.1 A 108dB-SNR 1.1mW Oversampling DAC with a Three-Level DEM Technique

8:30 AM

K. Nguyen, A. Bandyopadhyay, B. Adams, K. Sweetland, P. Baginski
Analog Devices, Wilmington, MA

A multi-bit audio DAC in a 0.18µm CMOS process uses a three-level DEM scheme and an ISI-free output stage to achieve 108dB SNR while consuming a total of 1.1mW per channel from a 1.8V supply.

27.2 A 0.7V 36µW 85dB-DR Audio ΔΣ Modulator Using a Class-C Inverter

9:00 AM

Y. Chae, I. Lee, G. Han
Yonsei University, Seoul, Korea

An audio ΔΣ modulator is realized in a standard 0.18µm CMOS process, exploiting the possibility of substituting a class-C inverter for an OTA. The measurement results from the fabricated chip demonstrate 81dB SNDR, 84dB SNR, and 85dB DR for a 20kHz signal bandwidth. The chip consumes 36µW from a 0.7V supply.

27.3 An Inverter-Based Hybrid ΔΣ Modulator

9:30 AM

R. Veldhoven, R. Rutten, L. Breems
NXP Semiconductors, Eindhoven, Netherlands

A hybrid ΔΣ modulator with 1st-order analog filter, 5b quantizer, 2nd-order digital filter, 1b quantizer, and 1b DAC is presented. The active circuitry is implemented solely with inverter circuits and standard digital cells. The 65nm CMOS modulator achieves a peak SNR of 77dB in 200kHz. Power consumption is 950µW at 1.2V and the area is 0.03mm^2.

Break 10:00 AM

27.4 A Noise-Coupled Time-Interleaved ΔΣ ADC with 4.2MHz BW, -98dB THD, and 79dB SNDR

10:15 AM

K. Lee[1], J. Chae[1], M. Aniya[2], K. Hamashita[2], K. Takasuka[2], S. Takeuchi[2], G. Temes[1]
[1]Oregon State University, Corvallis, OR
[2]Asahi Kasei, Atsugi, Japan

A two-channel time-interleaved noise-coupled ΔΣ ADC is realized in 0.18µm CMOS technology. Time interleaving doubles the effective clock rate while noise coupling raises the effective order of the noise-shaping loops, implements dithering, and also prevents tone generation in all loops. Using a 1.5V supply, the device achieved SFDR>100dB, THD = -98dB, and an SNDR of 79dB in a 4.2MHz signal band.

27.5 A 28mW Spectrum-Sensing Reconfigurable 20MHz 72dB-SNR 70dB-SNDR DT ΔΣ ADC for 802.11n/WiMax Receivers

10:45 AM

P. Malla[1,2], H. Lakdawala[1], K. Kornegay[3], K. Soumyanath[1]
[1]Intel, Hillsboro, OR
[2]Cornell University, Ithaca, NY
[3]Georgia Institute of Technology, Atlanta, GA

A reconfigurable MASH 2-2 ΔΣ ADC, fabricated in 90nm CMOS, has an OSR of 10.5 and uses a 1.2V supply. It achieves SNRs of 72, 62, 60, and 54dB with a 20MHz BW while consuming 28, 20, 15, and 12mW, respectively. The configuration and, therefore, power are determined by signal and blocker power. SNRs of 73, 77, and 78dB are achieved for BWs of 10, 5, 2.5MHz, respectively.

27.6 A 100mW 10MHz-BW CT ΔΣ Modulator with 87dB DR and -91dBc IMD

11:15 AM

W. Yang, W. Schofield, H. Shibata, S. Korropati, A. Shaikh, N. Abaskharoun, D. Ribner
Analog Devices, Wilmington, MA

A 5th-order CT ΔΣ modulator with a hybrid feedback-feedforward topology and 9-level quantization is implemented in a 0.18µm CMOS process. When clocked at 640MHz, the modulator achieves 87dB DR, 82dB peak SNDR, and -91dBc IMD over a 10MHz BW. The modulator occupies 0.7mm^2 and consumes 100mW from a 1.8V supply.

27.7 A 65nm CMOS CT ΔΣ Modulator with 81dB DR and 8MHz BW Auto-Tuned by Pulse Injection

11:45 AM

Y-S. Shu[1], B-S. Song[1], K. Bacrania[2]
[1]University of California, San Diego, CA
[2]Conexant Systems, Palm Bay, FL

Active filters for CT ΔΣ modulators are calibrated by injecting a binary pulse dither and nulling it with an LMS algorithm. A 3rd-order 4b prototype in 65nm CMOS occupies 0.5mm^2 and consumes 50mW at 1.3V. At 256MS/s (OSR=16), the DR is 81dB with a 2.4V_{pp} full-scale range. SNR and SNDR at -1dBFS are 76 and 70dB, respectively.

27.8 A CT ΔΣ ADC for Voice Coding with 92dB DR in 45nm CMOS

12:00 PM

L. Doerrer, F. Kuttner, A. Santner, C. Kropf, T. Puaschitz, T. Hartig
Infineon, Villach, Austria

A 2nd-order CT multi-bit (4b) ΔΣ ADC for voice coding is implemented in a 45nm CMOS process. The input operational amplifier is chopped to eliminate flicker noise and offset. The quantizer, a power-efficient 3-comparator tracking ADC with a capacitive voltage reference DAC, is suitable for low-voltage designs and high clock rates. Over a bandwidth of 20kHz, the DR is 86dB. The ADC consumes 1.2mW from a 1.1V supply when clocked at 12MHz.

Conclusion **12:15 PM**

NON-VOLATILVE MEMORY & DIGITAL CLOCKING

Chair: Mark Bauer, Intel, Folsom, CA

Associate Chair: Suhwan Kim, Seoul National University, Seoul, Korea

28.1 A 16Gb 3b/Cell NAND Flash Memory in 56nm with 8MB/s Write Rate

1:30 PM

Y. Li[1], S. Lee[1], Y. Fong[1], F. Pan[1], T-C. Kuo[1], J. Park[1], T. Samaddar[1], H. Nguyen[1], M. Mui[1], K. Htoo[1], T. Kamei[1], M. Higashitani[1], E. Yero[1], G. Kwon[1], P. Kliza[1], J. Wan[1], T. Kaneko[2], H. Maejima[2], H. Shiga[2], M. Hamada[2], N. Fujita[2], K. Kanebako[2], E. Tam[1], A. Koh[1], I. Lu[1], C. Kuo[1], T. Pham[1], J. Huynh[1], Q. Nguyen[1], H. Chibvongodze[1], M. Watanabe[1], K. Oowada[1], G. Shah[1], B. Woo[1], R. Gao[1], J. Chan[1], J. Lan[1], P. Hong[1], L. Peng[1], D. Das[1], D. Ghosh[1], V. Kalluru[1], S. Kulkarni[1], R. Cernea[1], S. Huynh[1], D. Pantelakis[1], C-M. Wang[1], K. Quader[1]

[1]Sandisk, Milpitas, CA

[2]Toshiba Semiconductor, Yokohama, Japan

A 16Gb 8-level NAND flash chip in 56nm CMOS is fabricated. 8MB/s write performance is achieved, comparable to previously published 4-level NAND performance. This chip provides a significant cost reduction compared to 4-level NAND flash in the same technology.

28.2 An 8KB EEPROM-Emulation DataFLASH Module for Automotive MCU

2:00 PM

S. Kawai, A. Hosogane, S. Kuge, T. Abe, K. Hashimoto, T. Oishi, N. Tsuji, K. Sakakibara, K. Noguchi

Renesas Technology, Itami, Japan

We describe an 8KB EEPROM-emulation DataFLASH module (E2FLASH) that replaces on-board EEPROM using dual-channel NOR-type flash memory cell (DCNOR), which has two separated channels. DCNOR is fabricated using existing processes and has high reliability by separating read channel and program channel structure. A module design is chosen as the suitable erase sequence and chip architecture for DCNOR. As a result, 8KB E2FLASH achieves program/erase (P/E) endurace over 1M cycles and 20ms/block erase time.

28.3 A 45nm 4Gb 3-Dimensional Double-Stacked Multi-Level NAND Flash Memory with Shared Bitline Structure

2:30 PM

K-T. Park, D. Kim, S. Hwang, M. Kang, H. Cho, Y. Jeong, Y-I. Seo, J. Jang, H-S. Kim, S-M. Jung, Y-T. Lee, C. Kim, W-S. Lee

Samsung Electronics, Hwasung, Korea

A 4Gb 3D double-stacked multi-level-cell NAND flash memory is developed using 45nm floating-gate CMOS with single-crystal-Si layer stacking. The 3D device stacks two Si layers that each contain 2Gb memory arrays with a cell size of 0.0021μm^2/b per unit feature area. A fully 3D architecture achieves 2.5MB/s with 2kB page size and 40μs read-access time, which are almost equivalent to conventional planar devices.

Break 3:00 PM

28.4 Resonant Global Clock-Distribution for the Cell Broadband-Engine™ Processor

3:15 PM

S. Chan[1], P. Restle[1], T. Bucelot[1], S. Weitzel[2], J. Keaty[2], J. Liberty[2], B. Flachs[2], R. Volant[3], P. Kapusta[4], J. Zimmerman[4]
[1]IBM T.J. Watson, Yorktown Heights, NY
[2]IBM, Austin, TX
[3]IBM, Hopewell Junction, NY
[4]IBM, Essex Junction, VT

The transformation of the global clock on the 90nm Cell Broadband Engine™ processor into a resonant clock, operating up to 5GHz, enables a resonantly clocked high-performance microprocessor. An existing processor design is retrofitted with a 1.2µm-thick Cu metal layer to implement 830 1.2nH on-chip spiral inductors. The measured global-clock power savings is up to 25% compared to non-resonant chips from the same wafer lot (approximately 5% of total chip power is saved when running actual workloads).

28.5 A Low-Jitter 8-to-10GHz Distributed DLL for Multiple-Phase Clock Generation

3:45 PM

K-J. Hsiao, T-C. Lee
National Taiwan University, Taipei, Taiwan

We demonstrate a distributed DLL with low jitter and high phase accuracy for multiphase clock generation. The frequency of operation ranges from 8 to 10GHz. The measured RMS jitter is 293.3fs and the maximum phase mismatch is 1.4ps. The distributed DLL occupies 0.03mm^2 active area in a 90nm CMOS technology and draws 15mA from a 1.0V supply.

28.6 A Modular All-Digital PLL Architecture Enabling Both 1-to-2GHz and 24-to-32GHz Operation in 65nm CMOS

4:15 PM

A. Rylyakov[1], J. Tierno[1], D. Turker[2], J-O. Plouchart[1], H. Ainspan[1], D. Friedman[1]
[1]IBM T.J. Watson, Yorktown Heights, NY
[2]Texas A&M University, College Station, TX

A 65nm CMOS modular ADPLL has two digital PLLs using distinct DCO designs for widely separated frequency ranges. In the PLLs, a common digital circuit controls the oscillator, a 1-to-2GHz 5-stage ring DCO in one and a 24-to-32GHz LC-tank DCO in the other. The common block uses the same 8b adder for the loop filter, the $\Delta\Sigma$ modulator, and the divider. The ring-DPLL has a second $\Delta\Sigma$ modulator for operation as a fractional-N synthesizer. The phase noise of the LC-DPLL at a 1MHz offset from 32GHz is -97dBc/Hz. The period jitter of the ring-DPLL at 2GHz is 1ps$_{rms}$.

28.7 A 9.5GHz 6ps-Skew Space-Filling-Curve Clock Distribution with 1.8V Full-Swing Standing-Wave Oscillators

4:45 PM

M. Sasaki
Hiroshima University, Hiroshima, Japan

A 9.5GHz clock distribution network is prototyped using 6M 0.18µm CMOS. Twelve inductively loaded standing-wave oscillators are cascaded to form a continuous curve that completely fills a 2.2×2.2mm^2 chip area. The skew is 6.0ps and the jitter is 4.3ps. The total power consumption, including the final buffers, is 60% of conventional CMOS clock buffers.

Conclusion **5:15 PM**

TD: TRENDS IN COMMUNICATION CIRCUITS & SYSTEMS

Chair: Koji Kotani, Tohoku University, Sendai, Japan

Associate Chair: Christian Enz, Swiss Center for Electronics and Microtechnology, Neuchâtel, Switzerland

29.1 A 2.4GHz MEMS-Based Transceiver

1:30 PM

D. Ruffieux, J. Chabloz, C. Muller, F-X. Pengg, P. Tortori, A. Vouilloz
CSEM, Neuchatel, Switzerland

A heterodyne 2.4GHz low-power transceiver architecture, relying on high-Q MEMS devices to perform RF filtering, implements a RF DCO and a thermally compensated frequency reference. The synthesizer, featuring a quasi-direct IF modulator, and the receiver are integrated in a 0.18µm CMOS process and draws 7.5mA.

29.2 A 2GHz 52µW Wake-Up Receiver with -72dBm Sensitivity Using Uncertain-IF Architecture

2:00 PM

N. Pletcher, S. Gambini, J. Rabaey
University of California, Berkeley, CA

A 2GHz wake-up signal detector for wireless sensor network receivers is enabled by the combination of a high-Q MEMS front-end filter (BAW resonator) with an ultra-low-power free-running CMOS ring oscillator acting as the RF LO. The heterodyne receiver with an energy-detection final downconversion consumes 52µW from a 0.5V supply and achieves -72dBm sensitivity at 100kb/s when implemented in 90nm CMOS.

29.3 A Fully-Integrated UHF Receiver with Multi-Resolution Spectrum-Sensing (MRSS) Functionality for IEEE 802.22 Cognitive-Radio Applications

2:30 PM

J. Park[1], T. Song[1], J. Hur[1], S. Lee[1], J. Choi[2], K. Kim[2], J. Lee[2], K. Lim[1], C-H. Lee[3], H. Kim[2,4], J. Laskar[1]
[1]Georgia Institute of Technology, Atlanta, GA
[2]Samsung Electro-Mechanics, Suwon, Korea
[3]Samsung RFIC Design Center, Atlanta, GA
[4]Hanbat National University, Daejeon, Korea

A spectrum-sensing energy detector integrated with a UHF receiver (470 to 862MHz) is fabricated in 0.18µm CMOS and occupies 4800×2400µm^2. The MRSS receiver including MRSS mode consumes about 300mW from a 1.8V supply. The minimum detectable sensitivity is -60dBm with 30dB dynamic range with 100kHz cos^4 window.

Break 3:00 PM

29.4 Advanced Planar Bulk and Multigate CMOS technology: Analog-Circuit Benchmarking up to mm-Wave Frequencies

3:15 PM

P. Wambacq, A. Mercha, K. Scheir, B. Verbruggen, J. Borremans, V. De Heyn, S. Thijs, D. Linten, G. Van der Plas, B. Parvais, M. Dehan, S. Decoutere, C. Soens, N. Collaert, M. Jurczak
IMEC, Heverlee, Belgium

The effect on analog/RF circuits of different options for CMOS downscaling beyond 45nm is investigated. Measurements on comparators, opamps and VCOs show high-speed potential for planar bulk CMOS with strain, and superior low-frequency analog performance for FinFETs.

29.5 Digital Detection of Oxide Breakdown and Life-Time Extension in Submicron CMOS Technology

3:45 PM

M. Acar, A-J. Annema, B. Nauta
University of Twente, Enschede, Netherlands

The lifetime of high-voltage analog circuits can be increased significantly by segmenting the power transistors into many smaller sections, all with their own breakdown detection circuitry, and switching off the sections with the most breakdowns. The concept is demonstrated on an RF PA realized in standard 90nm CMOS with 1.2V supply using only thin oxide transistors.

29.6 Superconductive Single-Flux-Quantum Circuit/System Technology and 40Gb/s Switch System Demonstration

4:15 PM

Y. Hashimoto[1], S. Nagasawa[1], T. Satoh[1], K. Hinode[1], H. Suzuki[1], T. Miyazaki[2], M. Hidaka[1], N. Yoshikawa[3], H. Terai[4], A. Fujimaki[5]
[1]International Superconductivity Technology Center, Tsukuba, Japan
[2]Japan Science and Technology Agency, Tsukuba, Japan
[3]Yokohama National University, Yokohama, Japan
[4]National Institute of Information and Communications Technology, Kobe, Japan
[5]Nagoya University, Nagoya, Japan

A superconductive single-flux-quantum (SFQ) 2×2 switch system demonstrates 40Gb/s port speed. The system has 32 10Gb/s I/Os and cools an SFQ switch MCM, containing a SFQ 2×2 switch chip and a superconductive voltage-amplifier chip, to 4K with a cryocooler. SFQ MUX/DEMUX integrated on the switch chip enables the switch to communicate with room temperature electronics at 40Gb/s. The switch, fabricated with a 10kA/cm^2 Nb process, consumes 0.51mW and has a switching time of <25ps.

29.7 A Wireless Dual-Link System for Sensor-Network Applications

4:45 PM

T. Kimura[1], H. Yano[1], Y. Aoki[1], N. Yoshida[1], J. Noda[2], T. Sukenari[2], Y. Konishi[2], T. Nakao[2], A. Mitsuhashi[2], D. Taguchi[1]
[1]NEC, Kawasaki, Japan
[2]NEC, Ikoma, Japan

A reduced-power-consumption ad-hoc multi-hop network system uses: (i) a Dual-Link communication scheme, which handles two different frequency bands (433MHz/2.4GHz) and sets optimum transmission for each application, providing data rates of 2.4kb/s and 6.144Mb/s, respectively, and (ii) a vine-tree network topology that offers low packet error rate without requiring a routing table for each node. Fabricated in 0.13µm RF CMOS, the die size is 5×5mm^2.

29.8 A 400µW 4.7-to-6.4GHz VCO under an Above-IC inductor in 45nm CMOS

5:00 PM

J. Borremans[1,2], P. Wambacq[1,2], M. Kuijk[2], G. Carchon[1], S. Decoutere[1]
[1]IMEC, Leuven, Belgium
[2]Vrije Universiteit Brussel, Brussels, Belgium

A 4.7-to-6.4GHz VCO is designed in 45nm bulk CMOS using an above-IC inductor on top of the active circuitry, yielding 28% area reduction. The inductor is shielded from the circuitry, using the top metal layers of the CMOS back-end, which enables low-cost fully integrated 3D IC realizations. The fully integrated VCO consumes 400µW, achieves a FoM of 185dB, and occupies 0.12mm^2.

Conclusion **5:15 PM**

DATA CONVERTER TECHNIQUES

Chair: Michael Flynn, University of Michigan, Ann Arbor, MI
Associate Chair: Kunihiko Iizuka, Sharp, Nara, Japan

30.1 An Over-60dB True Rail-to-Rail Performance Using Correlated Level Shifting and an Opamp with 30dB Loop Gain

1:30 PM

B. Gregoire, U-K. Moon
Oregon State University, Corvallis, OR

Correlated level shifting (CLS) is introduced as a technique to provide true rail-to-rail performance while reducing errors from finite opamp gain. There is no speed penalty. CLS is applied to a pipelined ADC that achieves 10.5 ENOB operating 16mV from rails using an opamp with 30dB loop gain and a 0.9V supply.

30.2 A 32mW 1.25GS/s 6b 2b/step SAR ADC in 0.13µm CMOS

2:00 PM

Z. Cao[1], S. Yan[1], Y. Li[2]
[1]University of Texas, Austin, TX
[2]Analog Devices, Wilmington, MA

A 1.25GS/s 6b ADC is implemented in a 0.13µm digital CMOS process by time-interleaving two SAR ADCs with 2.5GHz internal clock frequency, each converts 6 bits in 3 cycles. 5.5 ENOB at 1.25GS/s and 5.8 ENOB at 1GS/s are achieved without any external/off-line calibration, error correction, or post processing. The ADC consumes 32mW at 1.25GS/s including T/H and reference buffers, and occupies 0.09mm^2.

30.3 A 24GS/s 6b ADC in 90nm CMOS

2:30 PM

P. Schvan[1], J. Bach[2], C. Falt[1], P. Flemke[1], R. Gibbins[1], Y. Greshishchev[1], N. Ben-Hamida[1], D. Pollex[1], J. Sitch[1], S-C. Wang[1], J. Wolczanski[1]
[1]Nortel, Ottawa, Canada
[2]STMicroelectronics, Crolles, France

A 6b 24GS/s ADC is implemented in 90nm CMOS for 10-to-40Gb/s DSP-based optical receivers. An interleaved architecture of SAR-type self-calibrating converters operates from a 1V supply combined with an array of 2.5V T/Hs with delay, gain, and offset calibration capability. A 25mW 1.5GS/s sub-ADC results in total power consumption of 1.2W. ENOB is >4.1 up to 8GHz and >3.5 up to the Nyquist frequency.

Break 3:00 PM

30.4 A 1V 11b 200MS/s Pipelined ADC with Digital Background Calibration in 65nm CMOS

3:15 PM

K-W. Hsueh, Y-K. Chou, Y-H. Tu, Y-F. Chen, Y-L. Yang, H-S. Li
MediaTek, Hsinchu, Taiwan

A 1V 11b 200MS/s pipelined ADC is fabricated in a 65nm digital CMOS process and achieves 75dB SFDR and 62dB SNDR (10.04 ENOB). The ADC performance is enhanced by an on-chip digital background calibration circuit and its convergence time is reduced through succeeding stage output-code generators built in the pipelined stages. The 1.1mm^2 chip consumes 180mW from a 1V supply.

30.5 A 90nm 4.7ps-Resolution 0.7-LSB Single-Shot Precision and 19pJ-per-Shot Local Passive Interpolation Time-to-Digital Converter with On-Chip Characterization

3:45 PM

S. Henzler[1], S. Koeppe[1], W. Kamp[1], H. Mulatz[2], D. Schmitt-Landsiedel[2]
[1]Infineon, Munich, Germany
[2]Technical University Munich, Munich, Germany

The concept and on-chip characterization circuitry of a 90nm local passive interpolation TDC is presented. With an interpolation factor of 4, the resolution is 4.7ps at 1.2V with 0.7 LSB single-shot precision at 19pJ/shot power consumption. The measured INL and DNL are ±1.2 and ±0.6 LSB, respectively. Active compensation limits the error caused by $10ps_{rms}$ long-term clock jitter to ±1LSB.

30.6 A Clockless ADC/DSP/DAC System with Activity-Dependent Power Dissipation and No Aliasing

4:15 PM

B. Schell, Y. Tsividis
Columbia University, New York, NY

A fully clockless programmable ADC/DSP/DAC system is realized in a 90nm CMOS process and uses a 1V supply. The 8b voiceband system operates in continuous time, occupies $1.7mm^2$, has no aliasing, achieves an in-band SDR of 47 to 62dB and a power dissipation of 0.25 to 1.7mW, depending on input activity.

30.7 A Split-Load Interpolation-Amplifier-Array 300MS/s 8b Subranging ADC in 90nm CMOS

4:45 PM

Y. Shimizu, S. Murayama, K. Kudoh, H. Yatsuda
Sony LSI Design, Nagasaki, Japan

An 8b 300MS/s subranging ADC is implemented in a 90nm digital CMOS process. A split-load interpolation amplifier is used as a pre-amplifier for the comparators; it halves the number of parallel-connected pre-amplifiers and comparators, achieving greater efficiency in both area and power. The ADC can operate at up to 300MS/s with 7.2 to 7.9 ENOB. FOMs are 680fJ/conversion-step at 300MS/s from a 1.2V supply and 290fJ/conversion-step at 100MS/s from a 0.7V supply.

30.8 A 6b 0.2-to-0.9V Highly-Digital Flash ADC with Comparator Redundancy

5:00 PM

D. Daly, A. Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

A 6b highly digital flash ADC is implemented in a 0.18µm CMOS process. The ADC operates in the sub-threshold regime down to 200mV and employs comparator redundancy to improve resolution. Common-mode rejection is implemented digitally via an IIR filter. The minimum FOM of the ADC is 125fJ/conversion-step at a 0.4V supply, where it achieves an ENOB of 5.05 at 400kS/s.

Conclusion **5:15 PM**

RF & MM-WAVE POWER AMPLIFIERS

Chair: Satoshi Tanaka, Renesas Technology, Komoro, Japan
Associate Chair: Andreas Kaiser, IEMN-ISEN, Lille, France

31.1 TX and RX Front-Ends for the 60GHz Band in 90nm Standard Bulk CMOS

1:30 PM

M. Tanomura[1], Y. Hamada[2], S. Kisimoto[2], M. Ito[2], N. Orihashi[2], K. Maruhashi[2], H. Shimawaki[1]
[1]NEC, Otsu, Japan
[2]NEC, Kawasaki, Japan

A mm-wave direct-conversion TRX is implemented in standard 1V 90nm CMOS with careful consideration of reliability. The TX includes a PA, a VGA, a driver amplifier (DA) and an I/Q modulator. In the RX, two LNAs in series are followed by a VGA, a DA, and an I/Q demodulator. The PA uses 20Ω transmission lines in its low-loss output matching network. It achieves an output power of 8.4dBm with a power gain of 10.3dB, a PAE of 7.0%, and a linear gain of 15.2dB at a drain voltage of 0.7V. The complete TX achieves a 6.0dBm output power for a 2.6Gb/s QPSK signal.

31.2 A 60GHz 1V +12.3dBm Transformer-Coupled Wideband PA in 90nm CMOS

2:00 PM

D. Chowdhury, P. Reynaert, A. Niknejad
University of California, Berkeley, CA

A 60GHz two-stage 1V differential PA is designed in 90nm CMOS. It uses compact transformers for input, output, and interstage matching and has an area of 660×380μm^2. It achieves a 1dB compressed output power of 9dBm and a saturated power of 12.3dBm. Peak drain efficiency is 32% and peak PAE is 8.8%. The power gain at 60GHz is 5.5dB with 3dB bandwidth exceeding 22GHz.

31.3 60 and 77GHz Power Amplifiers in Standard 90nm CMOS

2:30 PM

T. Suzuki, Y. Kawano, M. Sato, T. Hirose, K. Joshin
Fujitsu Laboratories, Atsugi, Japan

60GHz and 77GHz PAs are implemented in standard 90nm CMOS. Critical signal loss is reduced by using matching networks with short stubs. A transistor model and its parameters are developed that enable the design of mm-wave circuits. The chips achieve saturated output powers of 10.6dBm (60GHz) and 6.3dBm (77GHz) from a 1.2V supply.

Break 3:00 PM

31.4 A Single-Chip WCDMA Envelope-Reconstruction LDMOS PA with 130MHz Switched-Mode Power Supply

3:15 PM

V. Pinon, F. Hasbani, D. Pache, A. Giry, C. Garnier
STMicroelectronics, Crolles, France

A single-chip envelope-reconstruction transmitter integrates a 1.95GHz PA and a 130MHz SMPS in 0.25μm BiCMOS process, in a 1.1mm^2 area. The PA exhibits an output power up to 27dBm for WCDMA signals and has 46% overall PAE. ACLRs of -39/-47dBc and rms EVM of below 4% are compliant with standard specifications.

31.5 A 28.6dBm 65nm Class-E PA with Envelope Restoration by Pulse-Width and Pulse-Position Modulation

3:45 PM

J. Walling[1,2], H. Lakdawala[2], Y. Palaskas[2], A. Ravi[2], O. Degani[2], K. Soumyanath[2], D. Allstot[1]
[1]University of Washington, Seattle, WA
[2]Intel, Hillsboro, OR

A class-E PA with on-chip pulse-width and pulse-position modulator (PWPM) for envelope restoration is fabricated in 65nm CMOS. The PA operates from a 2.5V supply and occupies 1.3×1.6mm^2. It achieves a measured P_{out} of 28.6dBm with a PAE of 28.5%. It can amplify phase-modulated signals and signals of limited peak-to-minimum ratios. It achieves rms EVM values of 1.2% and 4.6% for a GMSK signal with symbol rate of 270kHz and a π/4-DQPSK signal with symbol rate of 192kHz, respectively.

31.6 An Outphasing PA for a Software-Defined Radio Transmitter

4:15 PM

S. Moloudi[1], M. Youssef[1], M. Makhimar[1], K. Takinami[2], A. Abidi[1]
[1]University of California, Los Angeles, CA
[2]Matsushita, San Jose, CA

A programmable PA for a software-defined radio with 20dBm maximum output power operates based on the principle of outphasing. A switching scheme is designed to solve the problem of power combining in outphasing. The system is tested for GSM, EDGE, and WCMDA signals with 56%, 44%, and 30% efficiency, respectively.

31.7 A Fully-Integrated Quad-Band GSM/GPRS CMOS Power Amplifier

4:45 PM

I. Aoki, S. Kee, R. Magoon, R. Aparicio, J. Zachan, G. Hatcher, D. McClymont, A. Hajimiri
Axiom Microdevices, Irvine, CA

A fully integrated quad-band PA with integrated input and output matching and on-chip closed-loop power control and supply from 2.9 to 6V is implemented in standard 0.13µm CMOS. It uses a standard package with no oscillations, degradation, or failures for over 2,000 hours of operation at 6V and 135°C under a VSWR of 15:1 (all angles) and produces up to +35dBm of RF power with a PAE of 48%.

31.8 Balanced SiGe PA Module for Multi-Band and Multi-Mode Cellular-Phone Applications

5:15 PM

A. Scuderi, C. Santagati, M. Vaiana, F. Pidala, M. Paparo
STMicroelectronics, Catania, Italy

The integration of a 6×8mm^2 transmit power module for multi-mode (GSM/EDGE/WCDMA) and multi-band (850 to 900MHz and 1800 to 2100MHz) operation is presented. The module hosts printed matching networks, on-glass 90° combiner, directional couplers, low-pass filters, and 2 SiGe balanced PAs capable of envelope and power tracking operation. The module delivers 34.9/32.9dBm (PAE 54/45%) and 27/26dBm (PAE 32/30%) in GSM/DCS and WCDMA modes, respectively.

Conclusion **5:30 PM**

MEMS & SENSORS

Chair: Farrokh Ayazi, Georgia Institute of Technology, Atlanta, GA
Associate Chair: Christoph Hagleitner, IBM, Ruschlikon, Switzerland

32.1 A CMOS Temperature-to-Digital Converter with an Inaccuracy of ±0.5°C (3σ) from -55 to 125°C

1:30 PM

C. van Vroonhoven, K. Makinwa
Delft University of Technology, Delft, Netherlands

A CMOS temperature-to-digital converter is based on an electrothermal filter (ETF) whose near-linear temperature-dependent phase shift is read out by an integrated phase-domain ΔΣ modulator. The device-to-device spread is dominated by lithographic errors in the ETF and corresponds to an inaccuracy of ±0.5°C (3σ) from -55 to 125°C. The device is fabricated in a 0.7μm CMOS process and the ETF and ΔΣM each dissipate 2.5mW from a 5V supply.

32.2 A 1.5μW 1V 2nd-Order ΔΣ Sensor Front-End with Signal Boosting and Offset Compensation for a Capacitive 3-Axis Micro-Accelerometer

2:00 PM

M. Kämäräinen, M. Paavola, M. Saukoski, E. Laulainen, L. Koskinen, M. Kosunen, K. Halonen
Helsinki University of Technology, Espoo, Finland

A 2nd-order ΔΣ sensor front-end for a capacitive 3-axis micro-accelerometer is implemented in 0.25μm CMOS and uses a 1V supply. Signal boosting and offset compensation are used. The front-end occupies 0.49mm^2 and draws 1.5μA while sampling 3 proof masses, each at 4.096kS/s. 12b accuracy is achieved in a 1Hz signal BW. A ±2g capacitive 3-axis accelerometer has measured noise in the x, y and z directions of 917μg/√Hz, 791μg/√Hz and 704μg/√Hz.

32.3 A Mode-Matching ΔΣ Closed-Loop Vibratory-Gyroscope Readout Interface with a 0.004°/s/√Hz Noise Floor over a 50Hz Band

2:30 PM

C. Ezekwe, B. Boser
University of California, Berkeley, CA

A vibratory gyroscope readout interface exploits mode matching to reduce power dissipation. The interface ensures mode matching over PVT using background calibration, and addresses the challenges raised by mode matching by using a force-feedback architecture that is tolerant of spurious resonances. The interface is fabricated in 0.35μm CMOS and achieves a noise floor of 0.004°/s/√Hz over 50Hz while dissipating 1mW.

Break 3:00 PM

32.4 An RF MEMS Variable Capacitor with Intelligent Bipolar Actuation

3:15 PM

T. Ikehashi[1], T. Miyazaki[2], H. Yamazaki[1], A. Suzuki[2], E. Ogawa[1], S. Miyano[2], T. Saito[1], T. Ohguro[1], T. Miyagi[1], Y. Sugizaki[1], S. Hiura[1], T. Masunaga[1], N. Otsuka[2], H. Shibata[1], Y. Toyoshima[1]
[1]Toshiba, Yokohama, Japan
[2]Toshiba, Kawasaki, Japan

An RF MEMS variable capacitor module with intelligent bipolar actuation (IBA) is implemented in a driver IC to prevent stiction in electrostatic actuators. The IBA eliminates the dielectric charging of the electrostatic actuator by detecting the charge trapped in the dielectric film and reversing the electric field orientation if it exceeds a set threshold. No failure is observed up to 10^8 cycles at 85°C.

32.5 A Chopper-Stabilized Lateral-BJT-Input Interface in 0.6µm CMOS for Capacitive Accelerometers

3:30 PM

D. Zhao, M. Zaman, F. Ayazi
Georgia Institute of Technology, Atlanta, GA

A lateral-BJT-input read-out circuit in 0.6µm CMOS interfaced with a fully differential capacitive accelerometer achieves an output noise floor of -118dBV/√Hz at 3Hz. The IC uses chopper stabilization with a lateral-PNP-input switched-capacitor voltage amplifier to demonstrate a resolution of 6.3µg/√Hz at very low frequencies. With an area of 2mm^2, the IC consumes 3.75mW from a 3V supply. The in-run bias instability of the accelerometer is better than 24µg in 10hours.

32.6 Single-Chip CMOS Analog Sensor-Conditioning ICs With Integrated Electrically-Adjustable Passive Resistors

3:45 PM

L. Landsberger, O. Grudin, S. Salman, T. Tsang, G. Frolov, Z. Huang, M. Renaud, B. Zhang
Microbridge Technologies, Montreal, Canada

Single-chip analog sensor-conditioning circuits with integrated electrically adjustable passive resistors allow adjustments without the drawbacks of digital conditioning. Adding a rudimentary bulk-silicon cavity-etch to a standard 1µm CMOS process enables innovations for thermally isolated adjustable resistors. One circuit has a ±50% gain adjustment range, 0.1% of full-scale output precision, ±500mV offset adjustment range and the other has further TC-Offset and TC-Gain adjustments.

32.7 A 100µW 64×128-Pixel Contrast-Based Asynchronous Binary Vision Sensor for Wireless Sensor Networks

4:15 PM

N. Massari, M. Gottardi, S. Jawed
Fondazione Bruno Kessler - IRST, Trento, Italy

This 100µW 3.3V 64×128-pixel vision sensor for sensor network applications estimates and quantizes the local contrast to two levels at the pixel level. The time-adaptive embedded processing employs a charge-transfer mechanism and requires 770pJ/pixel with no DC power consumption. A frame is read out asynchronously in 147µs, dispatching the 7b column address of each asserted pixel with a maximum data rate of 80Mpixel/s, significantly reducing the chip activity at the interface.

32.8 A 16×16 CMOS Proton Camera Array for Direct Extracellular Imaging of Hydrogen-Ion Activity

4:45 PM

M. Milgrew, M. Riehle, D. Cumming
University of Glasgow, Glasgow, United Kingdom

A 16×16 CMOS proton camera array is designed for direct extracellular imaging of hydrogen-ion activity. The single-chip ion-sensitive FET (ISFET) sensor array is fabricated in a standard 0.35µm CMOS process. Each pixel includes a floating-electrode ISFET and has an area of 12.8×12.8µm^2. After matching, each ISFET pixel has a threshold of -1V, a linear operating range of 2V and a measured sensitivity of 46mV/pH. A cell bioassay is used to demonstrate the operation.

Conclusion **5:15 PM**

Embedded Power Management for IC Designers

Organizer: **Ian Galton**, *University of California, San Diego, CA*
Instructors: **Jonathan Audy**, *Analog Devices, San Jose, CA*
Vadim Ivanov, *Texas Instruments, Tucson, AZ*
Stefan Rusu, *Intel, Santa Clara, CA*
Seth R. Sanders, *University of California, Berkeley, CA*

OVERVIEW:

New generations of consumer electronics products consume less power than their predecessors, but the requirement of the power delivery keeps changing in the direction of lower voltage and higher current. Simultaneously, market pressures dictate that every new generation of a product provide increased functionality at reduced cost, and emerging applications such as RF ID tags and sensor networks require elimination of conventional power sources altogether. These trends have caused power management to be a critical issue in modern IC design. The switching regulators predominantly used for DC power conversion in battery-operated devices introduce switching noise as the current they supply is increased, whereas analog and mixed-signal circuits that use the power become increasingly sensitive to such noise as their supply voltages are decreased. Increasingly, multiple voltage domains, each with different load scenarios, must be supported. Moreover, cost minimization often requires as much of the power management circuitry as possible to be implemented in a highly scaled CMOS technology optimized for digital circuitry. Hence, techniques to convert and use power efficiently are essential for success. This short course explain the fundamental power management issues faced by IC designers and presents state-of-the-art circuit- and system-level techniques for power management. It is intended for both entry-level and experienced engineers.

To Register, please use the ISSCC 2008 Registration Form in the Advance Program Centerfold. **Sign-in** is at the San Francisco Marriott Hotel, Level B-2, beginning at 7:00AM on Thursday, February 7, 2008.

The Short Course is offered twice on Thursday, February 7: The first offering is scheduled for **8:00AM to 4:30PM**. The second offering is scheduled for **10:00AM to 6:30PM**.

DVD of the Short Course & Selected Referenced Papers: A DVD of the Short Course may be purchased at registration, or at the on-site registration desk. A substantial price reduction is offered to those who attend the course. The DVD is mailed approximately four months after the end of the conference. The DVD includes: (1) The visuals of the four Short-Course presentations in PDF format; (2) Audio recordings of the presentations along with written transcriptions; (3) Bibliographies of background papers for all four presentations; and (4) PDF copies of selected relevant background material and important papers in the field (10 to 20 papers per presentation).

OUTLINE:

Navigating the Path to a Successful IC Switching Regulator Design

Power management encompasses a large breadth of knowledge and expertise. Power solutions cover magnetics, applications, system architecture, and IC design, with needs for precision DC performance in the presence of large switching currents. IC design engineers often find themselves faced with covering all these system-level aspects of a project on their own. Creating a successful power-management solution requires navigating a path through this vast breadth of knowledge to provide a robust, cost-effective solution that meets the required performance criteria. A goal of this talk is to provide a fundamental understanding of switching regulators and their tradeoffs, and to layout a map for new IC switching regulator designers, by which to navigate this path. The talk is organized as a top-down approach to the decision and design task, and include real-world examples and experiences along the way.

Instructor: Jonathan Audy received his BSc Hons degree in Electronics Engineering from Chelsea College, London University, England, in 1985. He is currently a Principal Design Engineer in the portable power group at Analog Devices, in San Jose, CA. He holds upwards of 15 patents in IC design covering voltage references, temperature sensors, OTP memory, switching regulator circuits, etc. In 1985 he joined Precision Monolithics. (PMI) in London as a Test Engineer, and in 1987 he transferred to California as a Product Engineer. Shortly thereafter, PMI was acquired by Analog Devices, at which time he moved into IC Design. He has designed and co-designed over 20 commercially successful ICs, from voltage references to stand-alone buck regulators and mobile Pentium Processor switching regulators.

Circuit Techniques for Switching Regulators

The top-down design of switching regulators determines the system building blocks and their requirements and priorities. Circuit design of these blocks requires expertise in precision, high-speed, low-power/low-voltage techniques as well as in digital and mixed-signal circuits. Every new design sets new goals that are often not possible to achieve with traditional methodologies. When new circuits are created using prior solutions, undesirable problems and compromises at the system level often occur. In this talk the design procedure of the switching regulator's constituent blocks are discussed, starting from block requirements, leading to their structure and then to circuit solutions. Topics include: high- and low-side gate drivers; error amplifiers and comparators; reference, biasing, temperature protection; continuous inductor current measurement; comparators for synchronous rectification; charge pumps and gate drive voltage boosters; oscillators, delays, and pulse-width modulation.

Instructor: Vadim Ivanov received MS (1980) and PhD (1987) degrees in control systems in St. Petersburg, Russia, working on ASICs for sensors, servo systems and motor control for naval navigation. In 1996 he joined Burr-Brown, presently Texas Instruments, as senior member of technical staff, where he designed operational amplifiers, instrumentation amplifiers, power amplifiers, DC-DC converters, LDOs, and references. He holds 36 US patents on analog circuit techniques and has authored more than 30 technical papers and three books.

Power Reduction and Management Techniques for Digital Circuits

While transistor geometries continue to shrink every two years, the scaling of the operating voltage levels has slowed down significantly. At the same time, power efficiency has become a key competitive feature for all digital circuits, from server farms to mobile devices. These technology trends call for aggressive power management schemes to reduce heat dissipation and extend battery life. This talk presents an overview of power-reduction techniques for digital circuits, with specific examples from key industry players and academic research. These techniques include multiple clock and power domains, dynamic voltage and frequency scaling, power gating, as well as switching and leakage power reduction circuit implementations.

Instructor: Stefan Rusu received the MSEE degree from the Polytechnic University in Bucharest, Romania. His industry experience includes over 15 years with Intel and 6 years at Sun Microsystems. He is presently a Senior Principal Engineer in Intel's Enterprise Microprocessor Group leading the technology and special circuits design activities for the Xeon® MP Processors. He has authored over 75 papers on VLSI circuit technology and holds 30 U.S. patents. He is an IEEE Fellow, a member of the Technical Program Committee for ISSCC, ESSCIRC and A-SSCC conferences and an Associate Editor of the IEEE Journal of Solid-State Circuits.

Power/Energy for Autonomous and Ultra-Portable Devices

A representative challenge for a wireless sensor node is to enable a reliable 30-year maintenance-free lifetime, and to be continuously available. Supplying and managing electrical energy for this task is one of the key aspects in meeting such a challenge. This presentation evaluates the relative merits of various ambient energy sources, i.e., light, vibration, and thermal gradient/fluctuation, among others. Given a feasible energy source or set of sources, a representative energy management system needs to convert, store, and then meter out electrical energy. Power system architectures and key specifications for representative components are discussed. A range of integrated circuit power conversion circuit functions and solutions are outlined, including synchronous rectification at ultra-low-power levels, nano-amp quiescent current DC-DC conversion strategies, and overall strategies for obtaining very high efficiency over an ultra-wide operating range.

Instructor: Seth R. Sanders received the SB degrees in electrical engineering and physics and the SM and PhD degrees in electrical engineering from MIT in 1981, 1985, and 1989, respectively. He was a Design Engineer at the Honeywell Test Instruments Division, Denver, CO from 1981-83. Since 1989, he has been on the faculty of the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, where he is presently Professor. His research interests are in efficient power-conversion circuits and components, in design and control of electric machine systems, and in nonlinear circuit and system theory as related to the power electronics field. He is presently actively supervising research projects in the areas of renewable energy, and digital pulse-width modulation strategies and associated IC designs for power conversion applications. During the 1992 to 1993 academic year, he was on industrial leave with National Semiconductor, Santa Clara, CA. Seth Sanders received the NSF Young Investigator Award in 1993 and multiple Best Paper Awards from the IEEE Power Electronics and IEEE Industry Applications Societies. He has served as Chair of the IEEE Technical Committee on Computers in Power Electronics, and as a Member-at-Large of the IEEE PELS Adcom.

F4: Power Systems from the Gigawatt to the Microwatt – Generation, Distribution, Storage and Efficient Use of Energy

Co-Organizers: **Eugenio Cantatore,** *Eindhoven University of Technology, Eindhoven, Netherlands*
Siva Narendra, *Tyfone, Portland, OR*

Committee: **Anantha Chandrakasan,** *Massachusetts Institute of Technology, Cambridge, MA*
Christian Enz, *CSEM, Neuchâtel,Switzerland*
Takayasu Sakurai, *University of Tokyo, Tokyo, Japan*
Ken Shepard, *Columbia University, New York, NY*
Shuichi Tahara, *NEC, Tsukuba, Japan*
Chris Van Hoof, *IMEC, Leuven, Belgium*

Energy is the most important resource on our planet. At the global level, humankind has to cope with limited energy availability and the environmental impact of energy generation. Therefore efficient use of energy along with judicious distribution and storage to better use the generated energy is vital. More environment-friendly energy generation and scavenging technologies will play a significant role in continuing to meet the energy demands. Total available energy is especially scarce in mobile applications and in the emerging field of distributed micro-systems: every IC designer is thus continuously challenged to an increasingly more efficient use of energy, and energy awareness is becoming a key aspect of cutting-edge system design.

This forum presents the latest advancements in a broad spectrum of topics related to energy, ranging from global level issues to micro-power applications, through the words and the vision of recognized experts. The talks encompass a circuit-design focus with a system perspective, in an effort to give a comprehensive view of the energy problem today.

The Forum starts discussing energy generation and storage. **Vladimir Bulovic** (MIT) demonstrates how the use of nano-structured materials improves the efficiency of solar cells and lighting, **Chris Van Hoof** (IMEC) presents a range of devices able to scavenge mechanical and thermal energy available in the environment to power distributed micro-systems, and **Yuji Suzuki** (Tokyo U) presents micro-scale generators exploiting the chemical energy contained in hydrocarbon fuels. **Peter H.L. Notten** (Eindhoven U. and Philips) addresses the potential of future rechargeable batteries, for applications ranging from plug-in hybrid cars to integrated all-solid-state batteries. The second part of the forum will explore energy issues at large power levels. **Pietro Perlo** (FIAT) analyzes the advantages of forthcoming electric vehicles, focusing on system-level issues and the role of electronics in these cars, while **Kenneth M. Huber** (PJM) highlights technologies needed to achieve better electric grid control for efficient energy distribution. The last part of the Forum focuses on the efficient use of energy. **Seth Sanders** (UC Berkeley) examines the problem of power conversion, addressing challenges and examples at different power levels (mobile applications vs. microprocessors), **Anantha P. Chandrakasan** (MIT) discusses strategies for building energy-aware systems for mobile and ultra-low-power applications, and **Shekhar Y. Borkar** (Intel) investigates the challenge of achieving energy-efficient terascale computing.

This all-day forum encourages open exchange in a closed workshop. Attendance is limited and pre-registration is required. Coffee breaks and a lunch will be provided, to allow a chance for participants to discuss the issues and ask follow-up questions to the forum presenters.

Forum Agenda:

Time	Topic
8:00	Breakfast
8:20	**Introduction** **Eugenio Cantatore,** *Eindhoven University of Technology, Eindhoven, Netherlands*
8:30	**Nanostructured Materials in Efficient Lighting and Photovoltaic Structures** **Vladimir Bulovic,** *Massachusetts Institute of Technology, Cambridge, MA*
9:20	**Micro-Power Generation Using Thermal and Vibrational Energy Scavengers** **Chris Van Hoof,** *IMEC, Leuven, Belgium*
10:10	Break
10:30	**Fuel-powered Micro-Power Generators for Mobile Applications** **Yuji Suzuki,** *University of Tokyo, Tokyo, Japan*
11:20	**Rechargeable Batteries from Milliwatt to Kilowatt** **Peter H.L. Notten,** *Eindhoven University of Technology/Philips, Eindhoven, Netherlands*
12:10	Lunch
1:00	**The Role of Smart Systems Integration in the Forthcoming Electrical Mobility** **Pietro Perlo,** *FIAT, Orbassano, Italy*
1:50	**New Challenges and Solutions in Electric Grid Control** **Kenneth M. Huber,** *PJM, Norristown, PA*
2:40	Break
3:00	**The Ubiquitous Power-Conversion Challenge** **Seth Sanders,** *University of California Berkeley, Berkeley, CA*
3:50	**Energy-Aware Portable and Micro-Systems** **Anantha P. Chandrakasan,** *Massachusetts Institute of Technology, Cambridge, MA*
4:40	**Energy Management in Future Many-Core Microprocessors** **Shekhar Y. Borkar,** *Intel, Hillsboro, OR*
5:30	Conclusion

F5: Future of High-Speed Transceivers

Co-Organizers: **Robert Payne,** *Texas Instruments, Dallas, TX*
Jri Lee, *National Taiwan University, Taipei, Taiwan*

Committee: **Franz Dielacher,** *Infineon Technologies, Villach, Austria*
David Robertson, *Analog Devices, Wilmington, MA*
Sanroku Tsukamoto, *Fujitsu Laboratories, Kawasaki, Japan*
Bill Redman-White, *NXP Semiconductors, Southampton, UK*
Doug Smith, *SMSC, Austin, TX*

This Forum covers the system challenges and circuit solutions needed to address the ever-increasing bandwidth requirements of chip-to-chip, board-to-board, and system-to-system communications. As the speed of electrical I/Os exceeds 10Gb/s and the speed of optical fiber systems exceeds 40Gb/s, the limits of process, circuit, and package technologies are approached, requiring continuous innovation to build higher performance systems.

Various equalization techniques and their applications are described in detail. Attendees will learn the performance limits and tradeoffs of various equalization techniques including transmit pre-emphasis, linear receive equalizers, decision feedback equalizers (DFE), and analog-to-digital conversion (ADC) followed by digital signal processing (DSP). In addition, the design of clock-and-data-recovery circuits, transmitter circuits, and equalizer adaptation will be discussed. The overarching theme is the design of circuits to enable next-generation data rates in a multitude of systems.

The Forum starts with a presentation from **Jared Zerbe** (Rambus) who overviews the challenges designers face in current- and future-generation wireline transceivers. After covering the loss mechanisms present in electrical channels, practical circuit solutions to address current and future transceiver demands are described. In the second talk, **Thomas Toifl** (IBM) continues the discussion on electrical communications with a focus on design techniques enabling ultra-low-power and area-efficient receivers. Next, **Andy Joy** (Texas Instruments) describes the application of ADCs and DSP to the challenge of receiver equalization. System requirements and circuit solutions to meet the equalization and clock-and-data recovery demands of multi-Gb/s systems are covered. **Koichi Yamaguchi** (NEC) then discusses duo-binary signaling as an alternate approach to achieving high-performance communication across band-limited channels. Circuits that transmit, equalize/receive, and perform the clock-and-data recovery of duo-binary symbols are described. While the majority of the previous presentations focus on the loss portion of the SNR problem, the fifth presentation from **Joy Laskar** (Quellan) addresses noise. Specifically, active crosstalk-cancellation techniques and circuits are described in the context of both wireline and wireless receivers.

The next two speakers shift focus from electrical signaling to optical signaling. **Hirotaka Tamura** (Fujitsu) begins the discussion by covering the roadmap of high-speed I/Os and interconnection technology. The technology limitations of both circuits and packaging technology are described. The second half of this presentation is on the implementation of CMOS integrated circuits needed to interface electrical systems to the O/E and E/O circuitry. The final presenter, **Oscar Agazzi** (ClariPhy), cover the design of DSP-based transceivers for single- and multi-mode optical fibers, including DFE and maximum-likelihood sequence estimation (MLSE) receivers. The theoretical and practical aspects of an experimental transceiver are discussed.

The forum concludes with a 45-minute question and answer session with all seven of the presenters in a panel format with an opportunity to compare and contrast the proposed solutions.

Forum Agenda:

Time	Topic
8:00	Breakfast
8:45	**Introduction** **Robert Payne,** *Texas Instruments, Dallas, TX*
9:00	**High-Performance Wireline Equalization: Issues, Designs, and Tradeoffs** **Jared Zerbe,** *Rambus, Los Altos, CA*
9:45	**Design Techniques for Ultra-Low-Power and Compact Transceivers in CMOS** **Thomas Toifl,** *IBM Research, Zurich Research Laboratory, Rüschlikon, Switzerland*
10:30	Break
10:45	**Electrical Channel Equalization Using Analog-to-Digital Conversion and DSP** **Andy Joy,** *Texas Instruments, Northampton, Northants, United Kingdom*
11:30	**Duobinary Signaling in High-Speed Electrical Links** **Koichi Yamaguchi,** *NEC, Kanagawa, Japan*
12:15	Lunch
1:15	**Active Noise Cancellation Techniques for High Speed Communications** **Joy Laskar,** *Quellan, Atlanta, GA*
2:00	**IC Design for Optical Communications** **Hirotaka Tamura,** *Fujitsu Laboratories, Yokohama, Kanagawa, Japan*
2:45	Break
3:00	**DSP-Based Optical Transceivers for Electronic Dispersion Compensation of Single-Mode and Multimode Fibers** **Oscar E. Agazzi,** *ClariPhy Communications, Irvine, CA*
3:45	Panel Discussion
4:30	Conclusion

F6: Transistor Variability in Nanometer-Scale Technologies

Co-Organizers: **Ron Ho,** *Sun Microsystems, Menlo Park, CA*
Sam Naffziger, *AMD, Fort Collins, CO*

Committee: **David Blaauw,** *University of Michigan, Ann Arbor, MI*
David Harris, *Harvey Mudd College, Claremont, CA*
Sonia Leon, *Sun Microsystems, Santa Clara, CA*
Scott Taylor, *IBM, Austin, TX*

Transistor variability presents one of the most important and difficult challenges of nanometer-scale integrated circuits. This forum discusses variability in VLSI circuits and address topics from the detailed nature of variability to how to build variation-tolerant designs for 65nm and finer technologies. We will present an overview of the causes of variability; the impact of computational lithography (*i.e.*, resolution-enhancement) on design; the state of the art in variation-tolerant architectures, circuits, and SRAMs; and methodology techniques for dealing with variability. The talks will also highlight important unsolved research problems for the future.

Forum Agenda:

Time	Topic
8:00	Breakfast
8:45	**Introduction** **Ron Ho,** *Sun Microsystems, Menlo Park, CA*
9:00	**Overview of Process Variability** **Rich Klein,** *AMD, Austin, TX*
10:00	**Computational Lithography and its Impact on Design** **Lars Liebmann,** *IBM, Hopewell Junction, NY*
11:00	Break
11:15	**Variation-Tolerant Architectures** **Hisashige Ando,** *Fujitsu Laboratories, Kanagawa, Japan*
12:15	Lunch
1:15	**Variation-Tolerant Circuit Design** **Tanay Karnik,** *Intel, Hillsboro, OR*
2:15	**Variability and SRAM Design** **Mike Clinton,** *Texas Instruments, Dallas, TX*
3:15	Break
3:30	**Variation-Tolerant Analog- and Digital-Design Methodologies** **Larry Pileggi,** *Carnegie Mellon University, Pittsburgh, PA*
4:30	Panel Discussion
5:00	Conclusion

F7: Digitally Assisted Analog & RF Circuits

Organizer: **Andrea Baschirotto,** *University of Salento, Lecce, Italy*

Committee: **Dieter Draxelmayr,** *Infineon Technologies,Villach, Austria*
Peter Kinget, *Columbia University, New York, NY*
John Long, *TU Delft, Delft, Netherlands*
William Redman-White, *NXP Semiconductors, Southampton, UK*
Francesco Rezzi, *Marvell Semiconductors, Pavia, Italy*
David Robertson, *Analog Devices, Wilmington, MA*
Robert Bogdan Staszewski, *Texas Instruments, Dallas, TX*

This all-day forum is geared toward analog and RF designers who deal with deeply scaled CMOS technologies and new applications. Cost reduction and integration opportunities compel designers to use scaled CMOS technologies, enabling integration of large amounts of digital signal processing at low power consumption and small area. However, analog/RF designers face the stark reality of working with devices that, while blazingly fast, are not condusive to the tried-and-true circuit techniques and architectures that have enjoyed a decades-long run of success. This creates a pressing need for new architectures for the analog and RF interfaces that exploit the availability of large numbers of cheap digital devices to enhance the performance and mitigate the poorer intrinsic device performance. This Forum gives a panorama of the key limitations to achieving high analog and RF performance and it proposes digital performance-enhancement techniques taking advantage of the availability of fast, small, and low power digital signal processing.

The Forum offers seven contributions from experts reporting theoretical analysis and experimental results for RF and analog interfaces based on digitally assisted approaches; there are talks on the circuit design of RF blocks (LNA, up/down conversion mixers, VCO, and PAs), on the analog and mixed-signal baseband blocks (analog filters, pipeline ADC, $\Delta\Sigma$ modulators, and sensor interfaces).

Larry Larson summarizes the digitally-enhanced linearization and efficiency-enhancement techniques for next generation RF systems. **Robert Staszewski** focuses on recently developed all-digital and digitally-intensive PLL architectures. The 'analog' content of these blocks is assisted by ultra-fast but inexpensive digital logic, which runs mostly automatically and in the background. **Joel Dawson** focuses on digitally assisted power amplifier linearization techniques. **Antonio Di Giandomenico** deals with wired telecommunications systems, discussing where and why digital-assistance is necessary and what are the advantages at system-level. **Maarten Vertregt** focuses on digitally enhanced analog in Nyquist converters, discussing in particular, the power/performance constraints. Starting from the application trends, he lists the performance limiting factors and proposes proper calibration techniques. **Robert Adams** gives an overview of mismatch-shaping and calibration techniques for D/A converters, including algorithms for dynamic element matching, mismatch-shaping and background self-calibration, which are ideally suited for implemenation in scaled technologies. Finally **Andrea Baschirotto** presents digitally-assisted solutions for large dynamic-range sensor interfaces.

Forum Agenda:

Time	Topic
8:00	Breakfast
8:20	**Introduction** **Andrea Baschirotto,** *University of Salento, Lecce, Italy*
8:30	**Digitally Assisted RF Front-End Technologies** **Larry Larson,** *University of California San Diego, CA*
9:20	**Digitally Assisted RF Frequency Synthesizers** **Robert Bogdan Staszewski,** *Texas Instruments, Dallas, TX*
10:10	Break
10:30	**Digitally Assisted and Hybrid Architectures for RF Transceivers in Deep-Submicron CMOS** **Joel L. Dawson,** *Massachusetts Institute of Technology, MA*
11:20	**Digitally Assisted Mixed-Signal Designs for Broadband Telecommunications Systems** **Antonio Di Giandomenico,** *Infineon Technologies, Villach, Austria*
12:10	Lunch
1:10	**Digitally Assisted Analog in Nyquist Converters: Solving Power/Performance Constraints** **Maarten Vertregt,** *NXP Semiconductors, Eindhoven, Netherlands*
2:00	**Can Sloppy Analog be Fixed by Smart Digital? An Overview of Mismatch-Shaping and Calibration Techniques for D/A Converters** **Bob Adams,** *Analog Devices, Acton, MA*
2:50	Break
3:10	**Digitally Assisted Large Dynamic-Range Sensor Interfaces** **Andrea Baschirotto,** *University of Salento, Lecce, Italy*
4:00	Panel Discussion – Moderator: **David Robertson**, Analog Devices
5:00	Conclusion

CONFERENCE REGISTRATION

ISSCC offers online registration. This is the fastest, most convenient way to register and will give you immediate confirmation of whether or not you have a place in the events of your choice. If you register online, which requires a credit card, your registration is processed while you are online, and your written confirmation can be downloaded and printed for your recordkeeping. To register online, go to the ISSCC website at www.isscc.org/isscc or go directly to the registration website at www.yesevents.com/isscc/index.asp

You can register by fax or mail using the 2008 IEEE ISSCC Advance Registration Form. There are two versions of the 2008 form: one for students and one for non-students. Make sure you use the correct form. All payments must be made in U.S. Dollars, by credit card or check. Checks must be made payable to "ISSCC 2008". It will take several days before you receive confirmation when you register using the form. **Registration forms received without full payment will not be processed until payment is received at YesEvents.**

Payments by credit card will appear on your monthly statement as a charge from ISSCC.

For those who wish to register by fax or mail, the Advance Registration Forms can be found at the center of this booklet. Please read the explanations and instructions on the back of the form carefully. Make sure you use the correct form.

The deadline for receipt of Early Registration fees is **January 4, 2008.** After January 4th, and on or before January 21, 2008, registrations will be processed only at the Late Registration rates. **After January 21st, you must register onsite.** Because of limited seating capacity in the meeting rooms and hotel fire regulations, **onsite registrations may be limited**. Therefore, you are urged to register early to ensure your participation in all aspects of ISSCC 2008.

Full conference registration includes one copy each of the Digest of Technical Papers in both hard copy and on CD and the ISSCC 2008 DVD that includes the Digest and Visuals (mailed in June). **Student registration does not include the ISSCC 2008 DVD, however the DVD is available for purchase at a reduced student rate.**

Special note for ISSCC 2008: To reduce the high cost and waste of producing and shipping the 800+ page Visuals Supplement book for all non-student attendees, this book is not included in conference registration for 2008. These visuals are included in the ISSCC 2008 DVD and the Visuals Supplement book is offered as an extra publication at a very low price, for those who still want to receive one.

All students must present their Student ID at the Conference Registration Desk to receive the student rates. Those registering at the IEEE Member rate must also provide their IEEE Membership number. Those individuals who are members of both IEEE and SSCS will also receive a complimentary copy of the SSCS Digital Archive DVD set for years through 2007.

The Onsite and Advance Registration Desks at ISSCC 2008 will be located in the Yerba Buena Ballroom Foyer at the San Francisco Marriott. All participants, except as noted below, must pick up their registration materials at these desks as soon as they arrive at the hotel. **Pre-registered Presenting Authors for each paper, and all pre-registered members of the ISSCC Program Committee, must go directly to Golden Gate A3 to collect their conference materials.**

The Digest of Technical Papers will be available for pick-up onsite beginning on Sunday at 4:00 PM, and during registration hours on Monday through Wednesday.

REGISTRATION HOURS:

Saturday, February 2	3:00 PM to 7:00 PM
Sunday, February 3	6:30 AM to 11:30 AM
	(Tutorial and Forum Attendees Only)
	11:30 AM to 8:00 PM
Monday, February 4	6:30 AM to 3:00 PM
Tuesday, February 5	8:00 AM to 3:00 PM
Wednesday, February 6	8:00 AM to 3:00 PM
Thursday, February 7	7:00 AM to 1:00 PM

NEXT ISSCC DATES AND LOCATION

ISSCC 2009 will be held on February 8-12, 2009 at the San Francisco Marriott Hotel.

FURTHER INFORMATION

Please visit the ISSCC website at www.isscc.org/isscc.
To be placed on the Conference Mailing List, please contact the Conference Office, c/o Courtesy Associates,

2025 M Street, N.W., Suite 800,
Washington, DC 20036
Email: ISSCC@courtesyassoc.com

HOTEL RESERVATIONS

ISSCC participants are urged to make their hotel reservations online. To do this, go to the conference website at www.isscc.org/isscc and click on the Hotel Reservation link to the San Francisco Marriott. **In order to receive the special group rates you will need to enter the following Group Codes: IEEIEEA for a single or double; IEEIEEB for a triple.** The special ISSCC group rates are $219/single; $219/double; and $239/triple (per night plus tax). All online reservations require the use of a credit card. Online reservations are confirmed immediately, while you are online. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC. Once made and confirmed, your online reservation can be changed by calling the Marriott at 415-896-1600 (ask for "Reservations"); or by faxing your change to the Marriott at 415-486-8153.

For those who wish to make hotel reservations by fax or mail, the Hotel Reservation Form can be found in the center of this booklet. Be sure to fill in your correct email address and fax number if you wish to receive a confirmation by email or fax. For those who must make hotel reservations by telephone, call 415-896-1600 and ask for "Reservations." **You must also provide the appropriate Group Code listed above when making your reservation.**

Reservations must be received at the San Francisco Marriott no later than January 11, 2008 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 11th, the group rate will no longer be available and reservation requests will be filled at the best available rate.**

IMPORTANT NOTICE FOR ALL 2008 ISSCC PARTICPANTS: It is vitally important that all 2008 ISSCC participants who do not live within driving distance of San Francisco make their hotel room reservations at the San Francisco Marriott, which is the conference hotel and location of all technical sessions and all other conference activities. The room rates have been negotiated based upon our need to use all available meeting space in the hotel. If we do not fill our negotiated room block, ISSCC must pay huge fees for using all of the space. This will then result in unnecessary and unpopular increases in registration fees for ISSCC in future years. Please support the Executive Committee in their attempt to keep your ISSCC registration fees reasonable. Book your room at the San Francisco Marriott hotel for ISSCC 2008.

CONFERENCE PUBLICATIONS

Additional ISSCC 2008 publications can be purchased at the Conference Registration Desks. Prices are lower for purchases collected onsite than for those publications ordered after the Conference that must be shipped to the purchaser for an additional fee. Following ISSCC 2008, please order publications by using the "Purchase ISSCC Conference Materials" link on the ISSCC website where you can order online or download an order form to mail or fax.

TECHNICAL BOOK DISPLAY AND STUDENT POSTERS

A number of technical publishers will have a collection of professional books and textbooks on display during the Conference. These books are available for sale or to order onsite. The Book Display is in the Golden Gate Hall C, located one level above the ballroom. The Book Display will be open on Monday from 12:00Noon - 6:30PM; on Tuesday from 10:00AM to 6:30PM; and on Wednesday from 10:00AM to 2:00PM.

The recent ISSCC/DAC and Asian Solid-State Circuits Conference (A-SSCC) student contest winners will display their work in poster form, outside Golden Gate C. **All these students will be available to explain their posters during the Social Hours on Monday and Tuesday evenings.**

ISSCC STUDENT FORUM

This year, at ISSCC 2008, a new initiative called the ISSCC Student Forum will take place on Saturday, February 2nd, at the San Francisco Marriott Hotel.

Audience attendance is limited and pre-registration is required.

The Forum consists of a succession of 5-minute presentations by graduate students (Masters and PhD candidates) from around the world, who have been selected on the basis of a short submission concerning their on-going research. Selection is based on the potential novelty and coherence of their proposed presentation. Note that the work described is not intended to be complete or final.

See www.isscc.org for the ISSCC Student-Forum Call for Participation.

AUTHOR INTERVIEWS

This year, Author Interviews will be held in the Ballroom Foyer outside Salons 1-6 and 10-15 on Monday through Wednesday. Social Hour refreshments will also be available in the Ballroom Foyer on Monday and Tuesday in addition to Golden Gate C and the Foyer surrounding the Book Display.

LUNCHEON FOR WOMEN IN SOLID-STATE CIRCUITS

Tuesday, February 5th, 12:00 Noon, The View Lounge – 39th floor

This year, ISSCC will sponsor a networking luncheon for women in solid-state circuits. It is an opportunity to get to know other women in the profession and discuss a range of topics including leadership, work-life balance, and professional development. Arathi Prabhakar, a General Partner at US Venture Partners, will be the keynote speaker. By registering and paying the nominal fee for this event, you will receive a ticket to the luncheon, as well as a chance to build new friendships and an opportunity to expand your professional network. Ladies, please indicate on your ISSCC registration form if you plan to attend this special event.

Arathi Prabhakar is a General Partner at US Venture Partners. From 1986-1993 she was a Program Manager and then a Director of DARPA. In 1993 she was appointed by President Clinton as Director of the National Institute of Standards and Technology (NIST) where she remained until 1997. She then joined Raychem serving as Senior VP and CTO, then served as VP and President of Interval Research Corporation. She received her B.S.E.E. from Texas Tech University and M.S. and Ph.D. from the California Institute of Technology. She is a Fellow of the IEEE.

UNIVERSITY EVENTS AT ISSCC 2008

Several universities are planning social events during the Conference. A link is provided during online registration that will take you to a list of universities where you can send an email to indicate your interest in attending. You can also reach this list directly by going to www.isscc.org/isscc and clicking on the "University Alumni Events" link.

SSCS DIGITAL ARCHIVE DVD SET

All ISSCC registrants who are also members of the IEEE Solid State-Circuits Society (SSCS) will receive a complimentary SSCS Digital Archive DVD Set. The two-DVD set contains the IEEE Journal of Solid-State Circuits (1966-2007) and the conference records of the ISSCC (1955-2007), the Symposium on VLSI Circuits (1988-2007), the Custom-Integrated-Circuits Conference (1988-2007), the Asian Solid-State Circuits Conference (2006), and the European Solid-State Circuits Conference (1997-2007).

- To add SSCS membership while renewing IEEE membership, go to www.ieee.org/renew
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Check-off boxes are provided on the registration form for ordering additional copies of the Digital Archive DVD.

CD OF THE ISSCC DIGEST AND DVD OF THE ISSCC DIGEST AND VISUALS SUPPLEMENT

Conference attendees will receive a complementary CD of the ISSCC 2008 Digest of Technical Papers in addition to the printed Digest at the Conference. This CD will allow easy access to an electronic version of the technical papers. In addition, all conference attendees (except student registrants) will receive (by mail) a complementary DVD containing the ISSCC 2008 Digest of Technical Papers and the ISSCC 2008 Visuals Supplement. **This DVD will be mailed by April 2008**.

ISSCC REPLAY ON DEMAND

This year, for the first time, ISSCC is offering a Web Access information service, called ISSCC Replay on Demand. Currently Replay on Demand is available for ISSCC 2007 and will be prepared for ISSCC 2008. While 2007 Replay is not separately available for sale, it will be included as part of the package for those that purchase ISSCC 2008 Replay on Demand. Meanwhile, a sample of ISSCC 2007 Replay is currently available for viewing at www.isscc.org. It includes a few selected papers. There you will find that the presentation for each paper consists of all presented visuals together with cursor overlay and audio recording of the speaker.

Those that purchase ISSCC Replay 2008 now, will be provided immediate personalized access privileges to the complete ISSCC Replay 2007. Replay 2008 will be available in June at which time notification will be sent.

ISSCC PRIOR-YEAR AND 2008 SHORT-COURSE DVDs

A DVD of the 2008 Short Course "Embedded Power Management for IC Designers" is available for purchase and **will be mailed in June 2008.** DVDs of prior Short Courses are also available:

- 2004: "Deep-Submicron Analog and RF Circuit Design"
- 2005: "RF CMOS Circuits"
- 2006: "Analog-to-Digital Converters"
- 2007: "Analog, Mixed-Signal and RF Circuit Design in Nanometer CMOS"

These DVDs contain audio and written transcripts synchronized with the presentation visuals. In addition, the DVDs contain a pdf of the presentations suitable for printing, and pdfs of key reference material. Check-off boxes are provided on the registration form for purchasing the DVDs.

ISSCC PRIOR-YEAR AND 2008 TUTORIALS DVDs

A DVD of the ten Tutorials at ISSCC 2008 is available for purchase and **will be mailed in June 2008.** A DVD of the ten Tutorials from ISSCC 2007 is also available. These DVDs contain audio and written transcripts synchronized with the presentation visuals. Check-off boxes are provided on the registration form for purchasing the DVDs.

MEMBERSHIP SAVES YOU ON ISSCC REGISTRATION.

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Be involved all year long.

You come to ISSCC once a year to network and keep informed about your field. Stay informed all year by joining the IEEE Solid-State Circuits Society. SSCS brings you

- The Archive DVD right now, a bonus when your register for ISSCC as an SSCS member, or join on site.
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Society membership costs $22 with IEEE membership. Use the onsite membership registration desk outside Golden-Gate to renew or join. This desk is staffed during the same hours as ISSCC registration desks.

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The simultaneous timing of papers given at ISSCC permits attendees to session-hop from session to session without having to miss important material. This Advance Program provides you with the starting time for each paper.

TAKING PICTURES, VIDEOS OR AUDIO RECORDINGS DURING ANY OF THE SESSIONS IS NOT PERMITTED

A printed supplement with speakers' visuals is no longer included in Conference registration. It is available for purchase at low cost and will be mailed in the Spring to those who select this option. The ISSCC 2008 DVD containing both the ISSCC 2008 Digest of Technical Papers and the visuals will be mailed by April to speakers and all non-student attendees. Student attendees can purchase this DVD at a reduced rate.

Conference Information:	Courtesy Associates email: ISSCC@courtesyassoc.com
Hotel Information:	San Francisco Marriott 55 Fourth Street San Francisco, CA 9410 Telephone: 415-896-1600
Press Information:	Kenneth C. Smith University of Toronto Phone: 416-418-3034 Fax: 416-971-2286 email: lcfujino@cs.com
Registration:	YesEvents P.O. Box 32862 Baltimore, MD 21282 Phone: 410-559-2236 or 1-800-937-8728 Fax: 410-559-2217 email: issccinfo@yesevents.com
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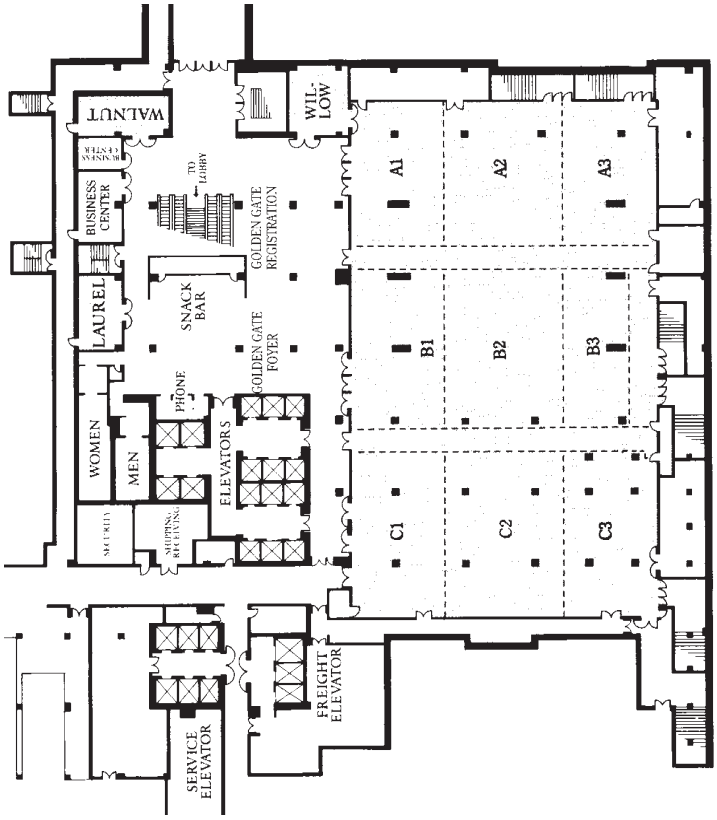
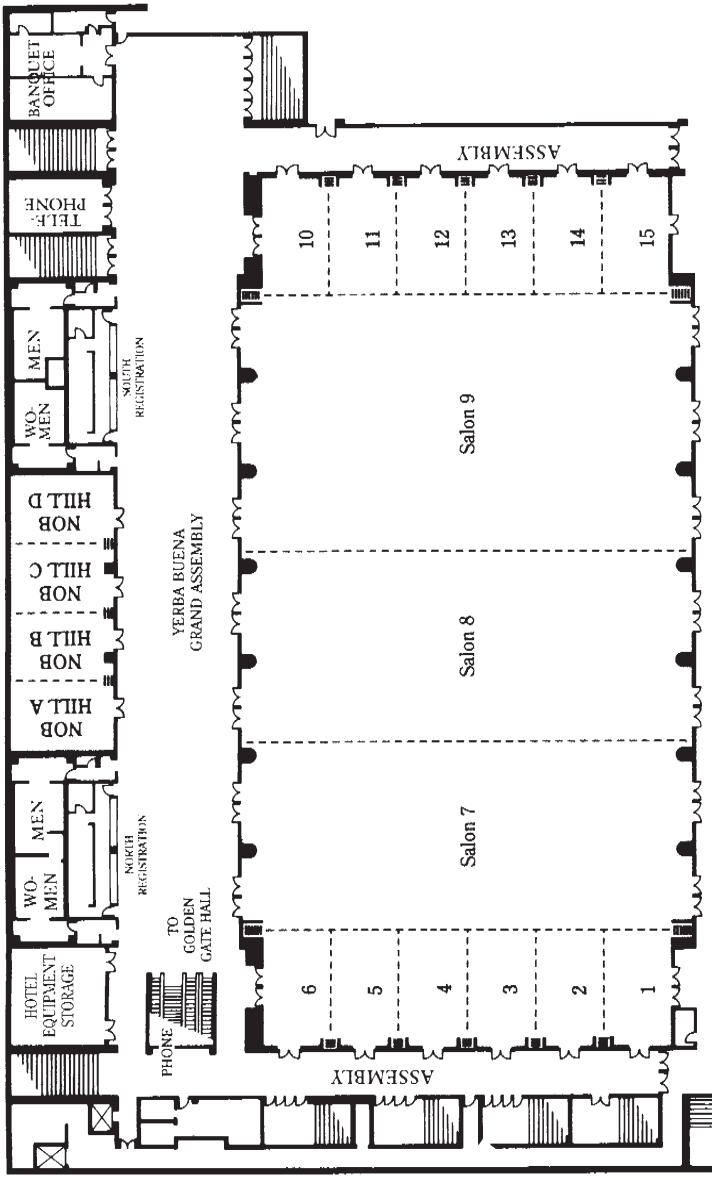
The Conference Book Display and Social Hour will be held in Golden Gate Hall. Layout appears below:

Golden Gate Hall
(B2 Level)



All Conference Technical Paper Sessions
are in the Yerba Buena Ballroom. Layout appears below:

Yerba Buena Ballroom
(Lower B2 Level)



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